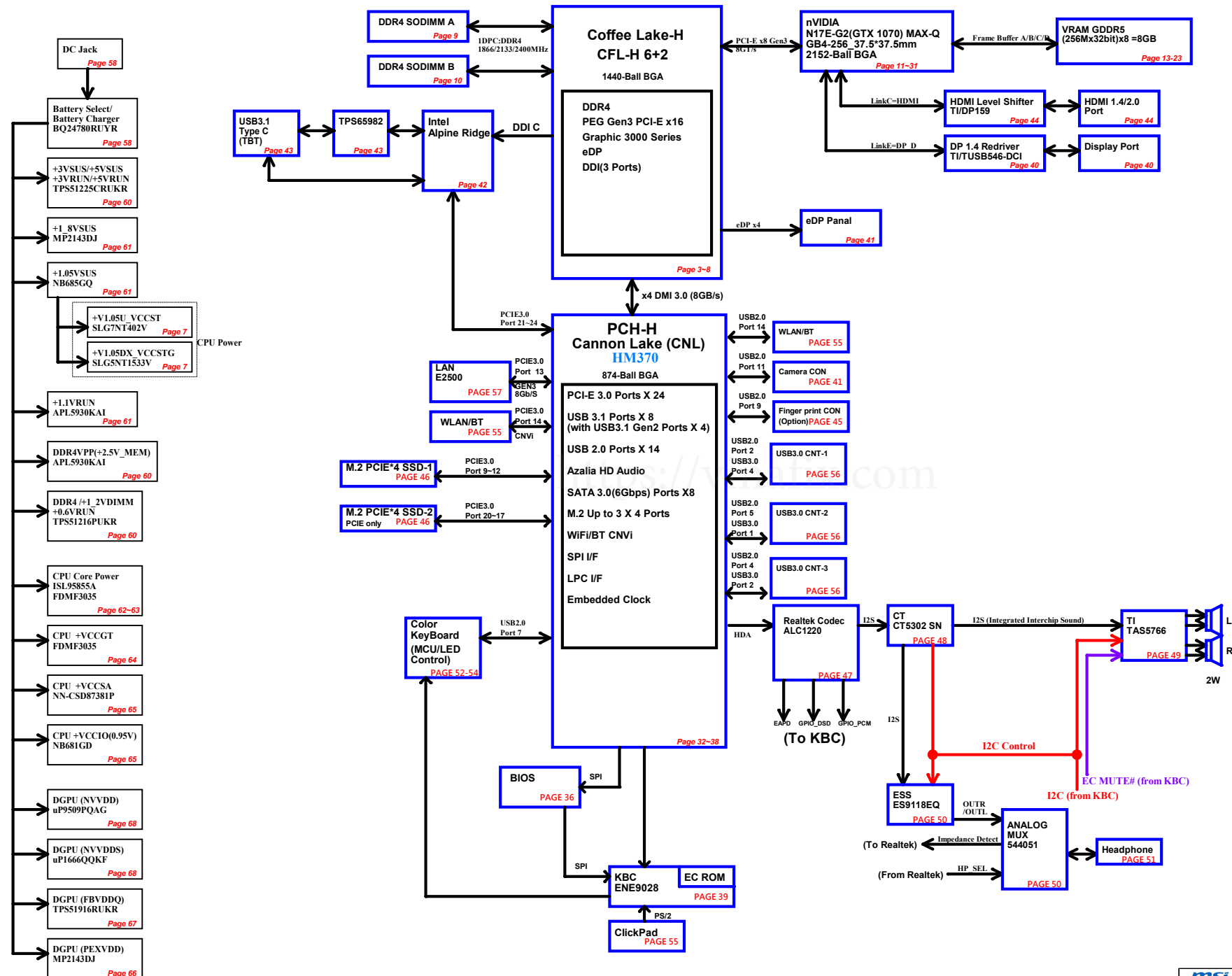


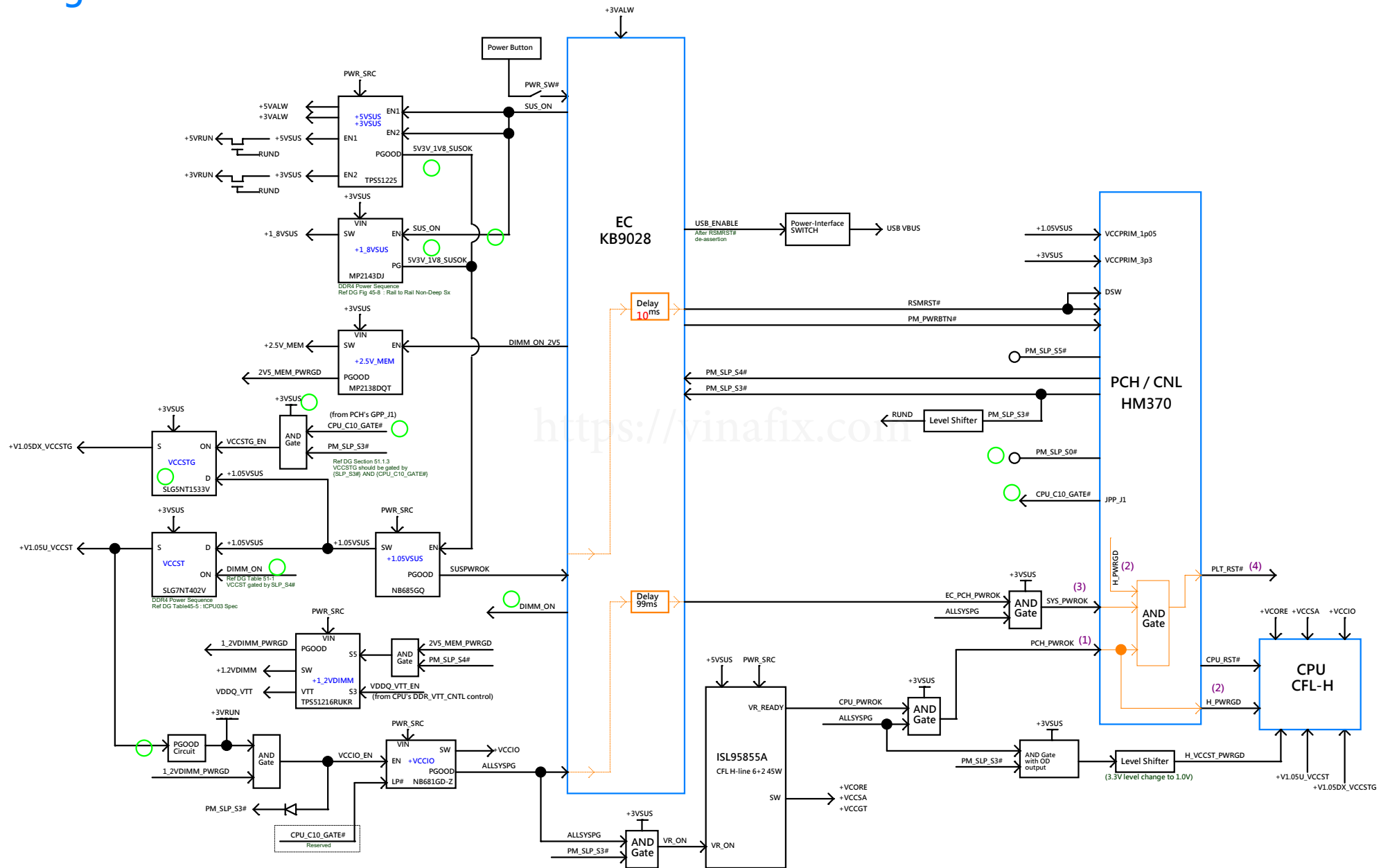
## Intel Coffee Lake-H





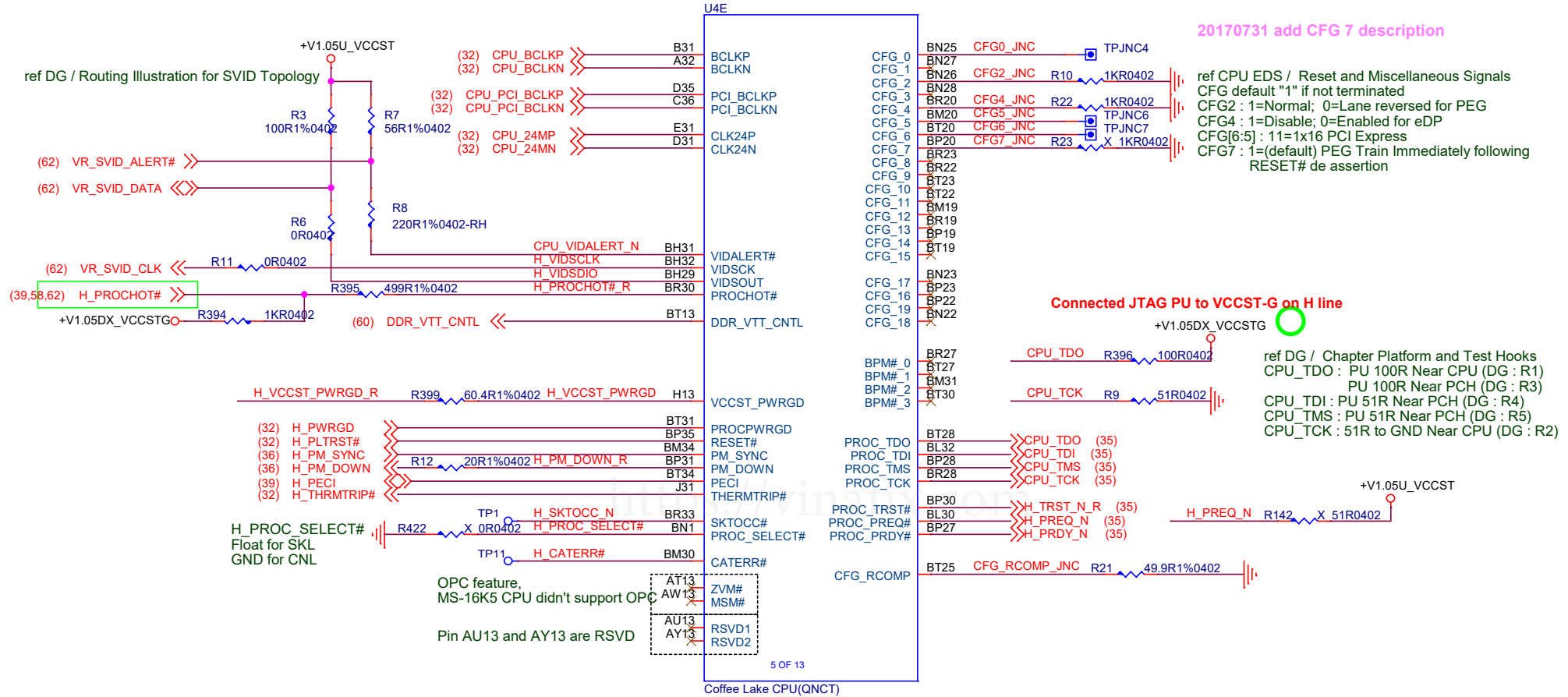
# MS-16K5 : CFL-H Mobile Power on Block

ref DG Chapter 4: Power Sequencing Spec  
Diagram

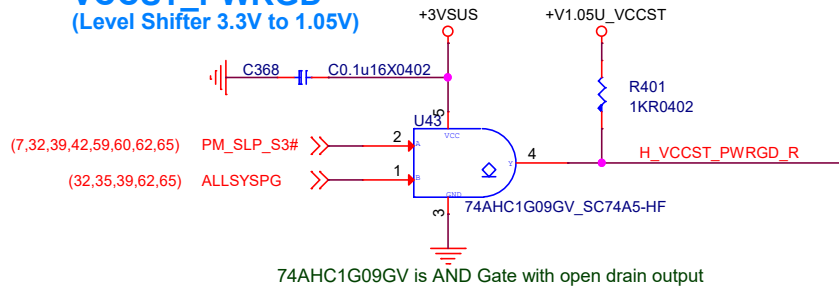




# CFL-H (HOST)



## VCCST\_PWRGD (Level Shifter 3.3V to 1.05V)

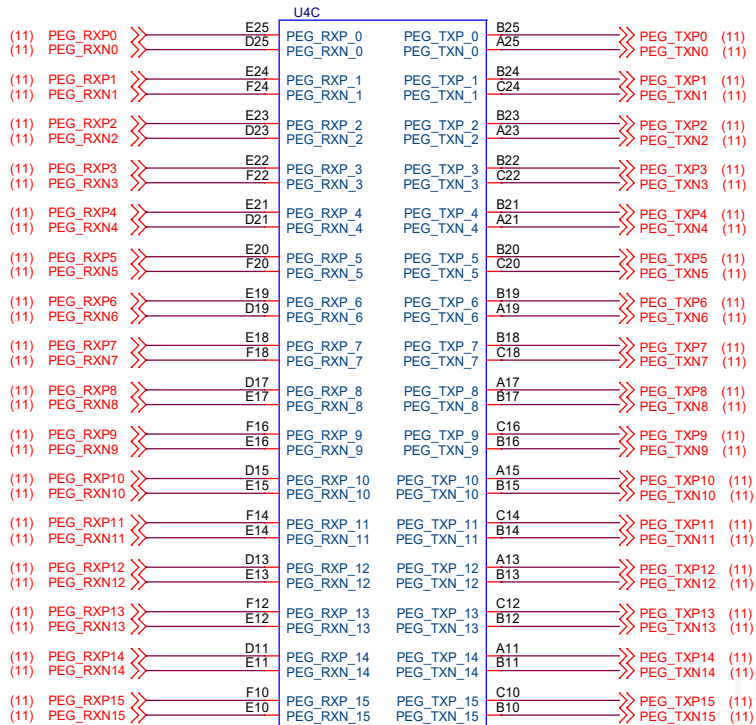




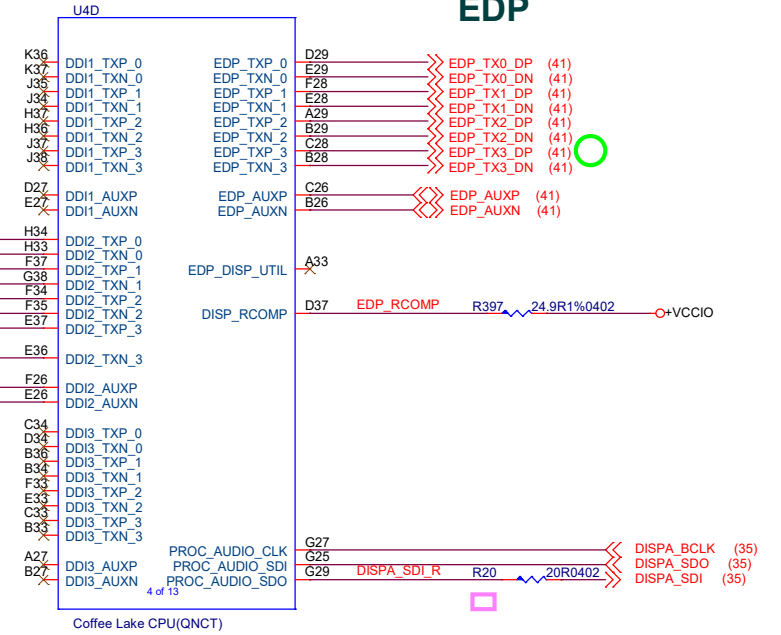
## DDR Channel B







DDI C  
DP to AR

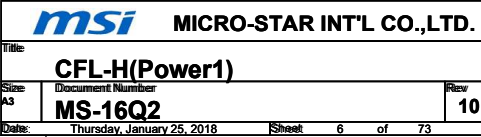


20170731 change R2351 to 20R to follow DG

3 OF 13  
Coffee Lake CPU(QNCT)

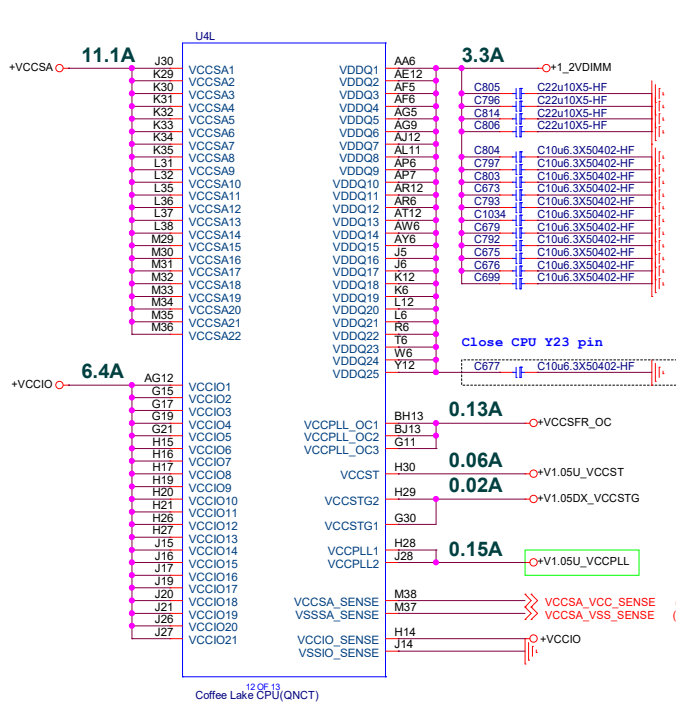
<b>msi</b> MICRO-STAR INT'L CO.,LTD.	
Title <b>CFL-H(DMI/Display)</b>	
Size Custom	Document Number <b>MS-16Q2</b>
Date: Thursday, January 25, 2018	Rev <b>10</b>
Sheet 5 of 73	



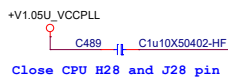
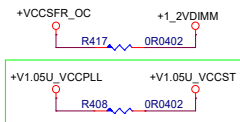




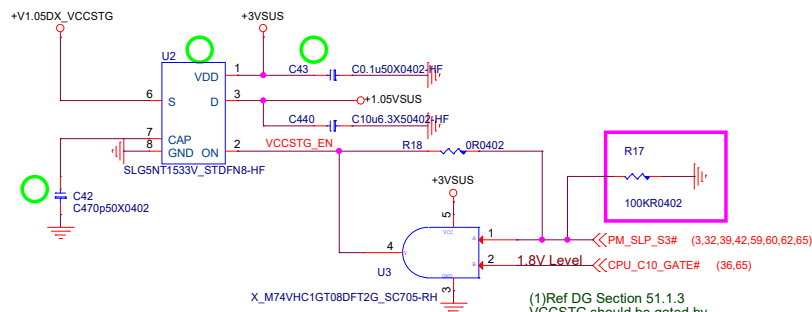
Follow CRB v0.7  
+VCCDU (+1.2V DIMM)  
4 x 22uF 0603  
12 x 10uF 0402



Remove +VCCVDDQ\_CLK, it combine with VDDQ.  
Pin number: Y12



## +V1.05DX\_VCCSTG



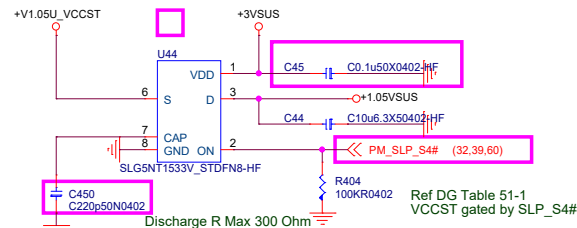
PN: T3E-1GT0800-005  
MC74VHC1GT08  
AND Gate Level Shifter

	VCC	Min	Max
VIH	3V	1.4V	
VIL	3V		0.53V

(1)Ref DG Section 51.1.3  
VCCSTG should be gated by  
(SLP\_S3#) AND (CPU\_C10\_GATE#)  
(2)Power Sequence spec tCPU26:  
CPU\_C10\_GATE# de-assertion to VCCSTG stable 10 < tCPU26 < 65 us

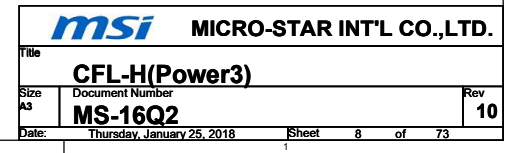
20170913 add R604 to follow DG

## +V1.05U\_VCCST



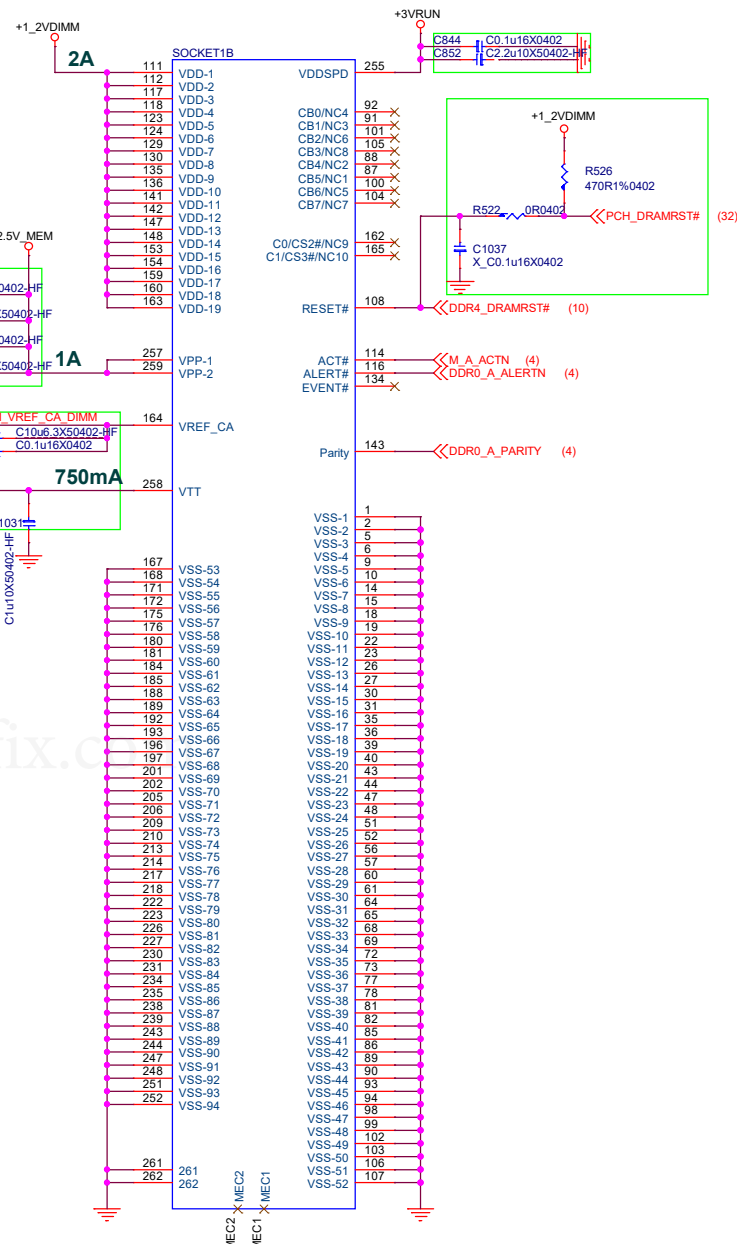
20170731 change C45 to 0.1uF  
20170804 change U39 to SLG5NT1533V to correct power sequence  
control by PM\_SLP\_S4#  
C404 change from 220pF to 220pF







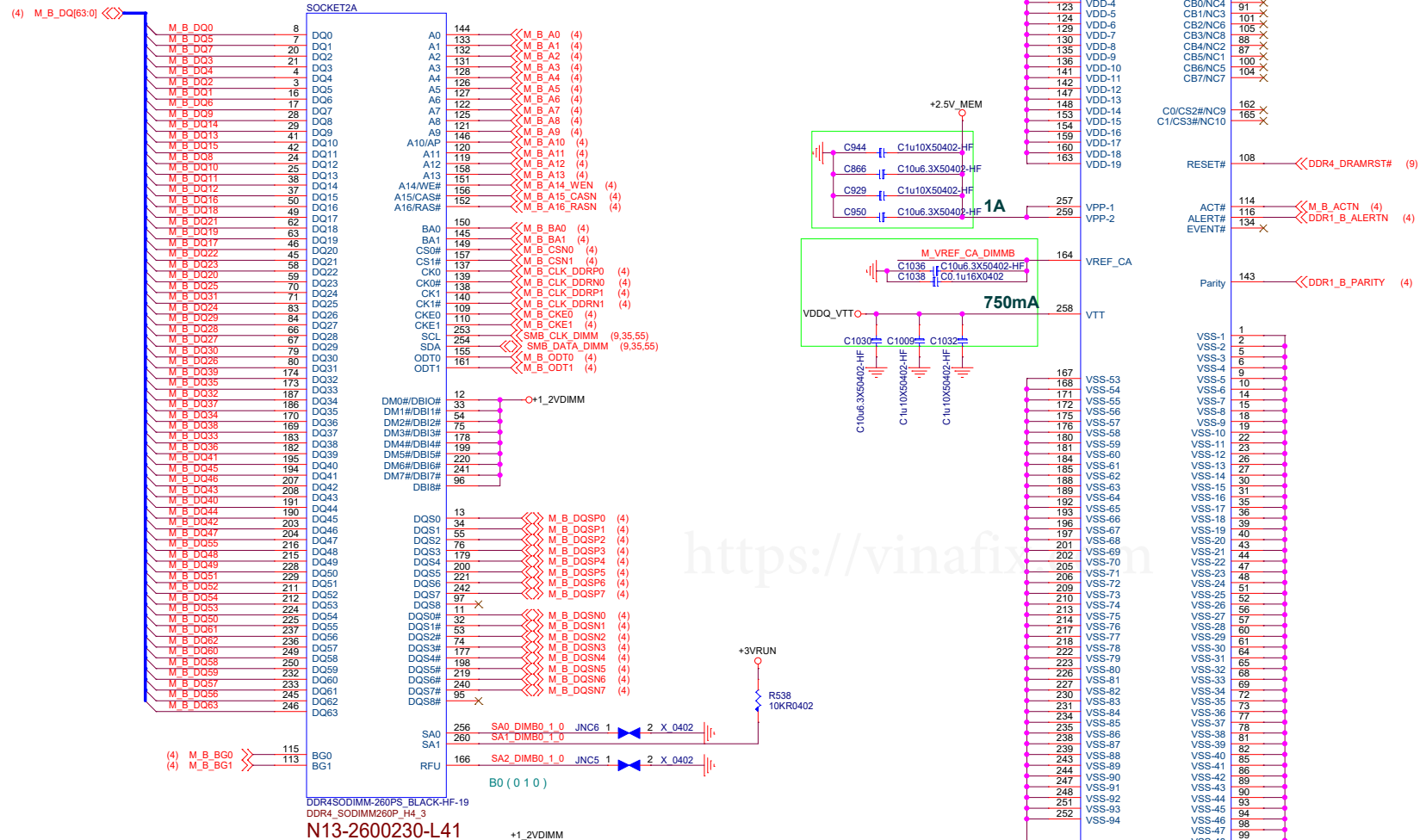
Vinafix.com



Size Custom	Document Number <b>MS-16Q2</b>	Rev <b>10</b>
Date:	Thursday, January 25, 2018	Sheet 9 of 73

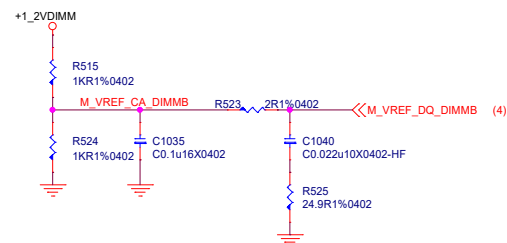
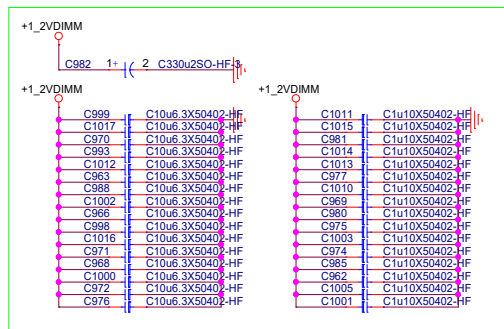



## SODIMM\_B0 (TOP-Standard)



20170912 C872 change to C71-33102AE-P01

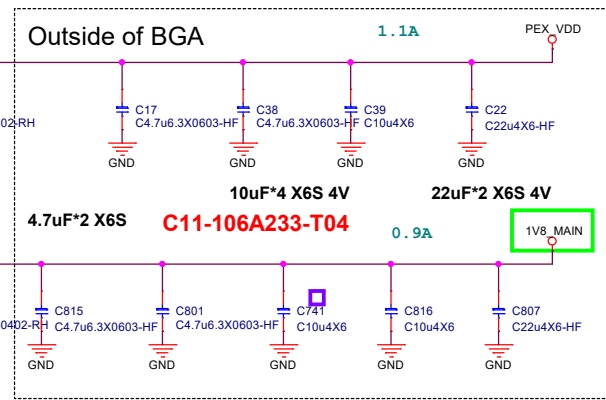
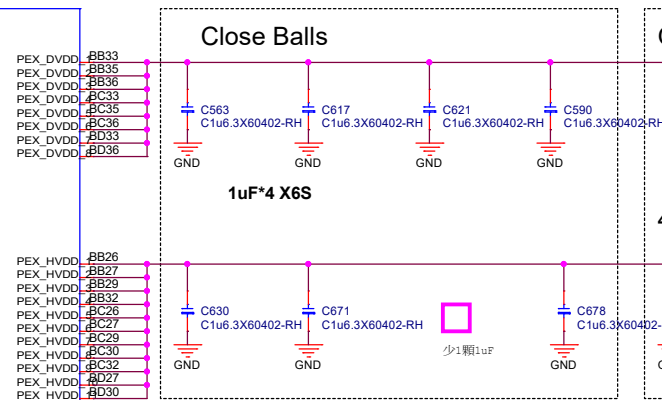
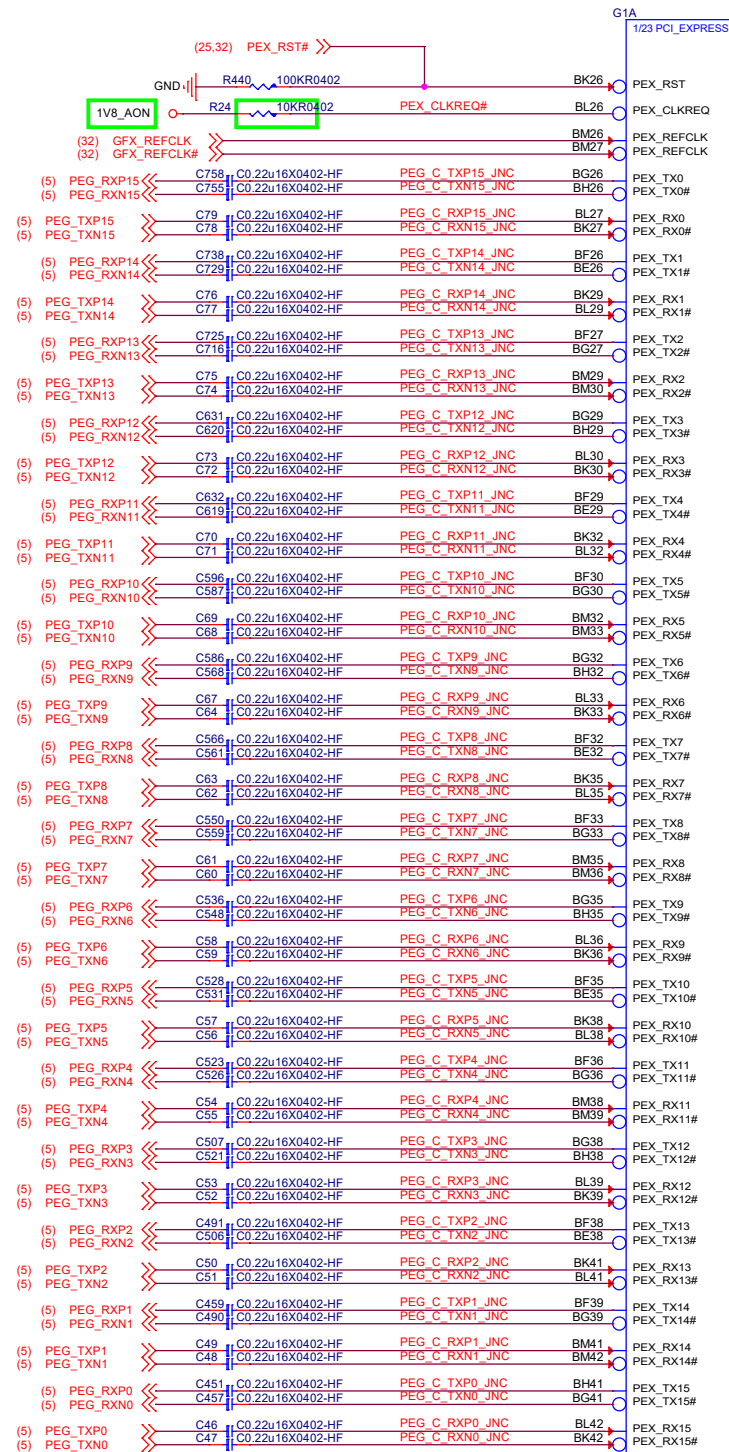
ref DG/ Section 4.14.1  
CFL-H DDR4 SDDIMM Power Plane Decoupling



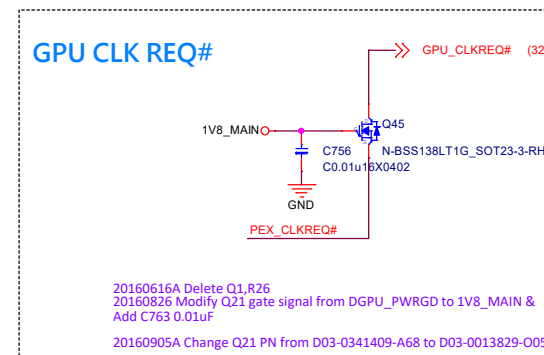
 <b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b> <b>DDR4 SODIMM_B0</b>	
<b>Size</b> <b>Custom</b>	<b>Document Number</b> <b>MS-16Q2</b>
<b>Date:</b> Thursday, January 25, 2018	
<b>Sheet</b> 10 <b>of</b> 73	
<b>Rev</b> 10	



# GPU PCI EXPRESS

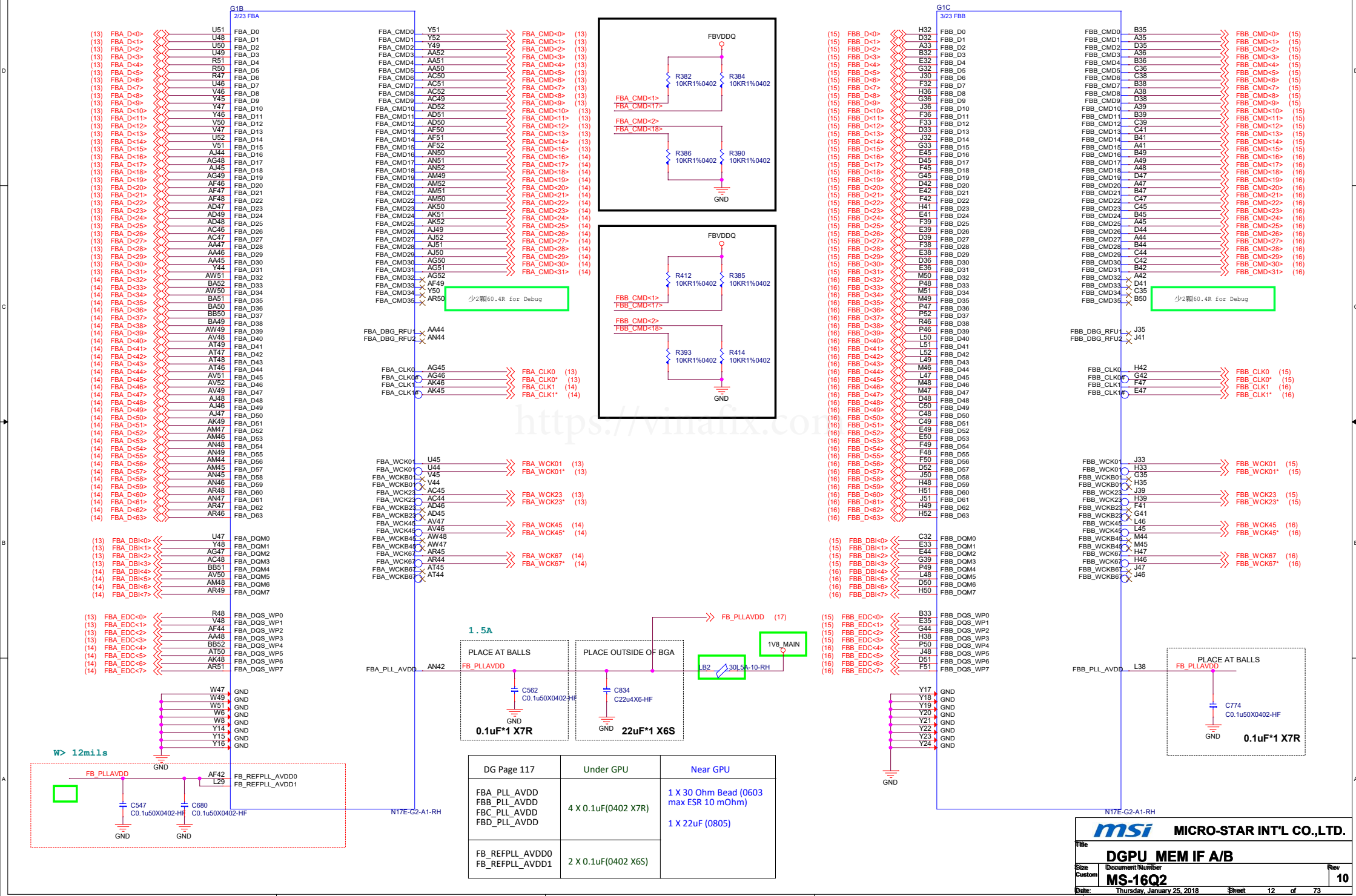


DG Page 117	Under GPU	Near GPU
PEX_HVDD	4 X 1uF(0402 X6S)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_DVDD	4 X 1uF(0402 X6S)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 1 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	1 X 0.1uF(0402)	





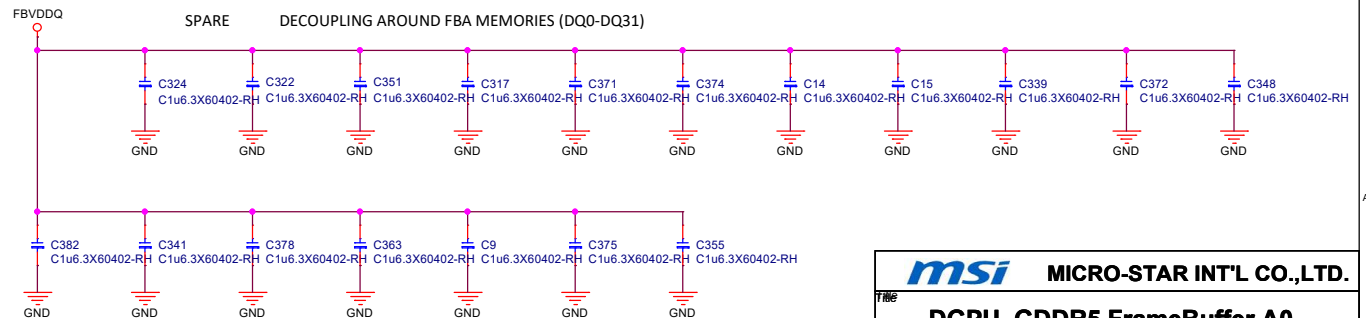
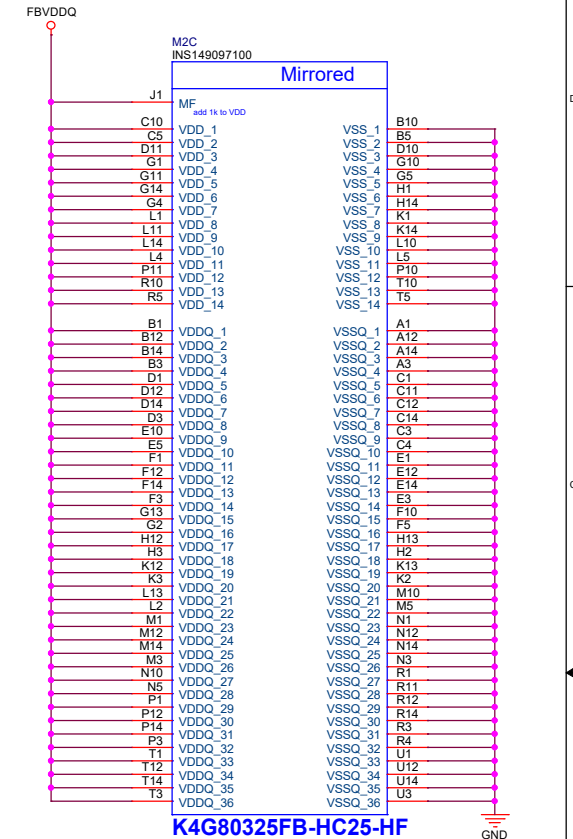
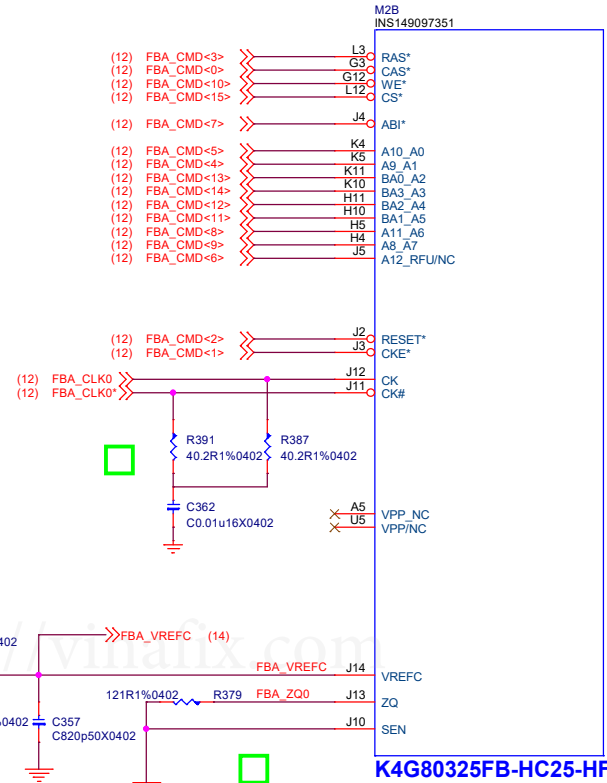
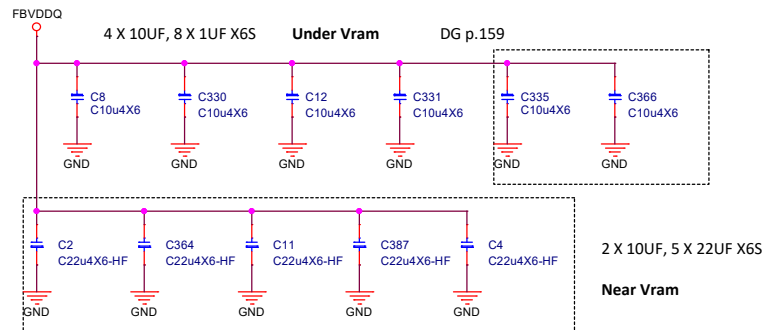
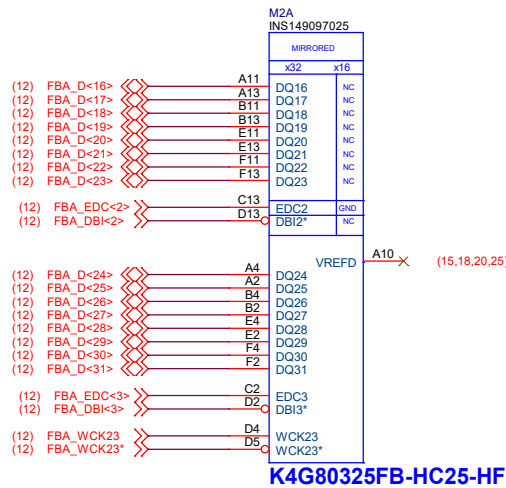
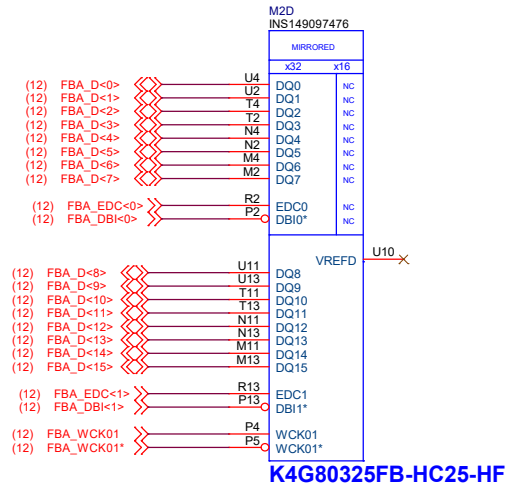
## GPU Frame Buffer Partition A/B





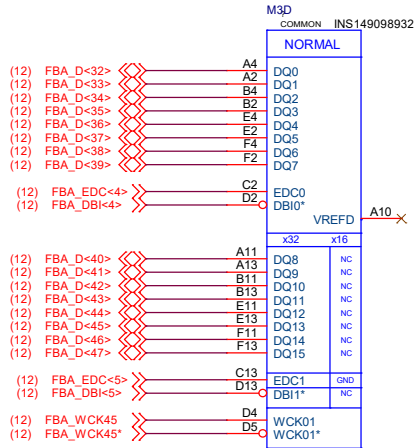
Hynix PN : M12-5GC2H05-H23 2G(64Mx32bit)  
Samsung PN : M12-2032585-S02 2G(64Mx32bit)

## DGPU\_GDDR5 FrameBuffer A0

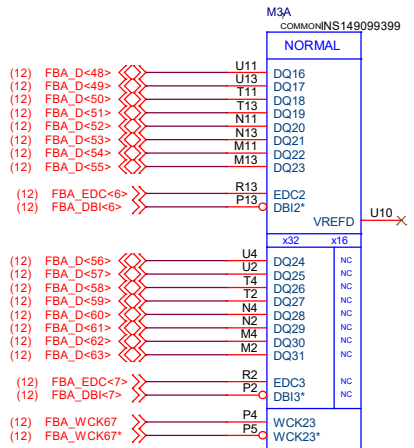




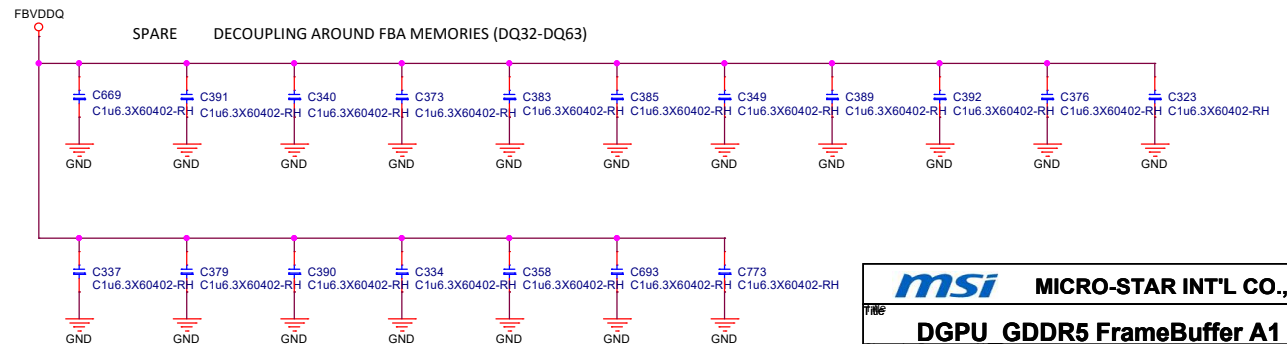
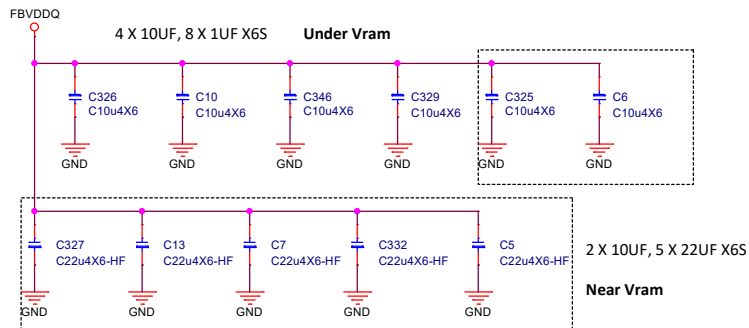
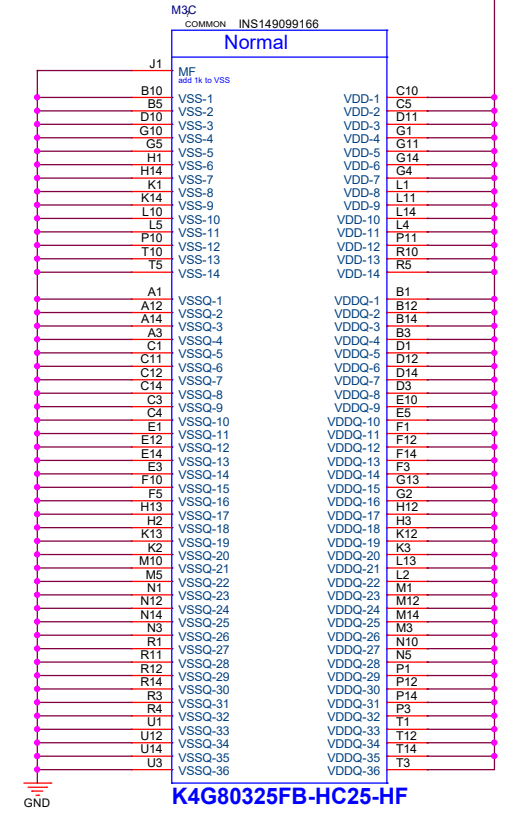
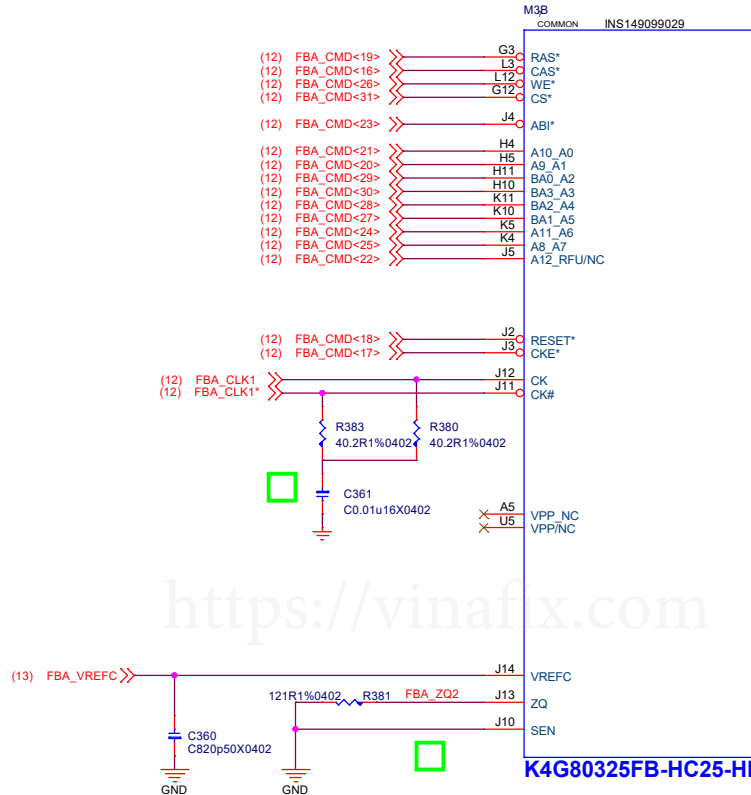
# DGPU\_GDDR5 FrameBuffer A1



K4G80325FB-HC25-HF

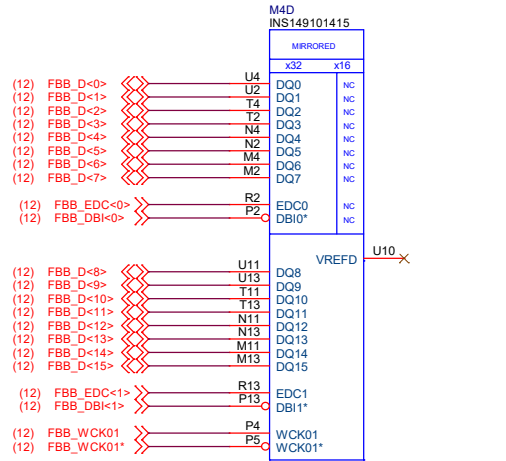


K4G80325FB-HC25-HF

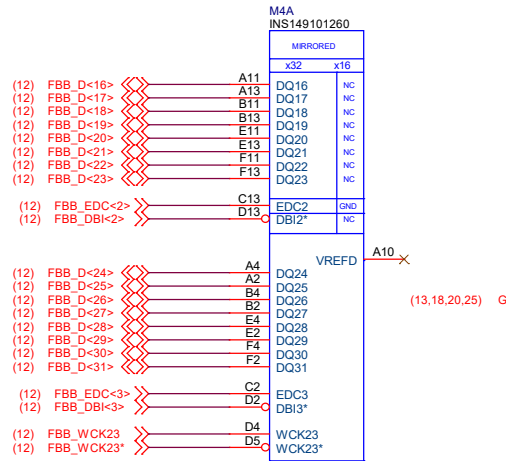




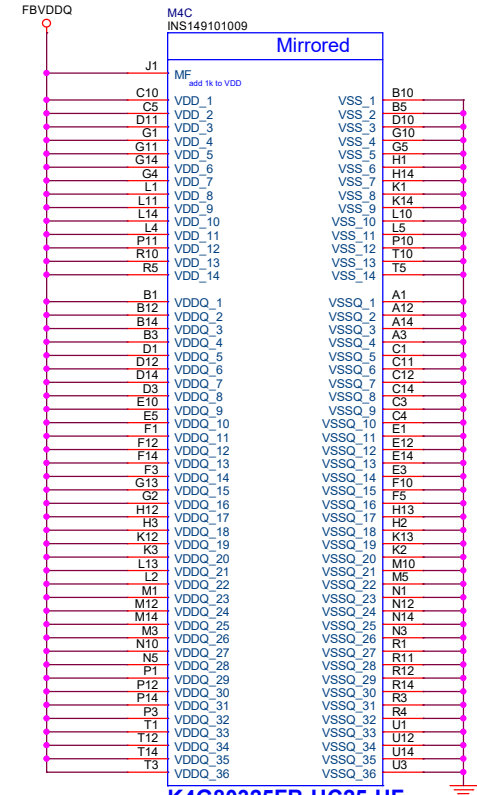
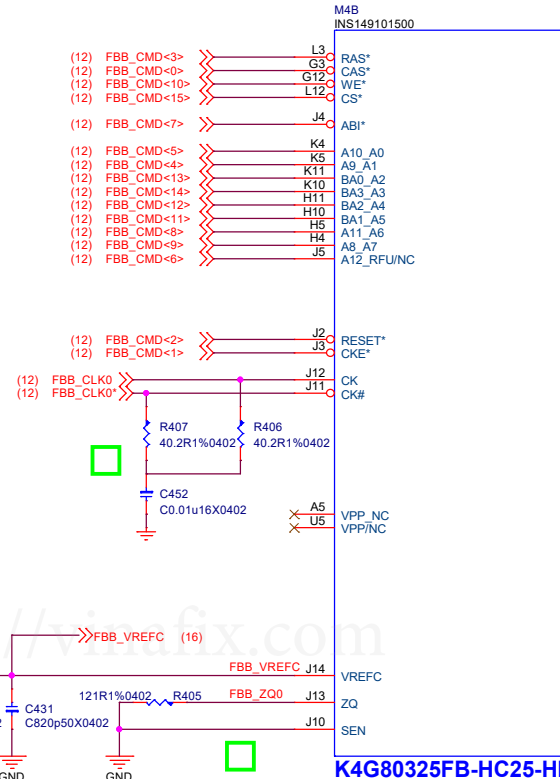
# DGPU\_GDDR5 FrameBuffer B0



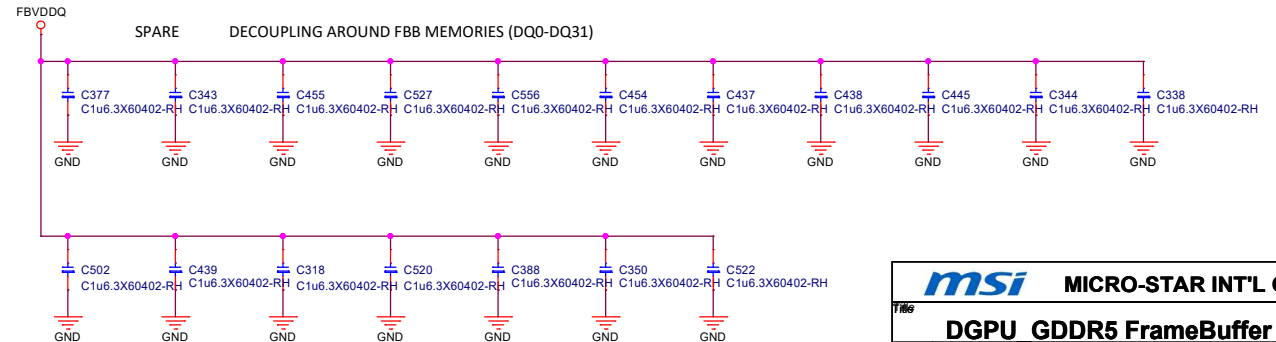
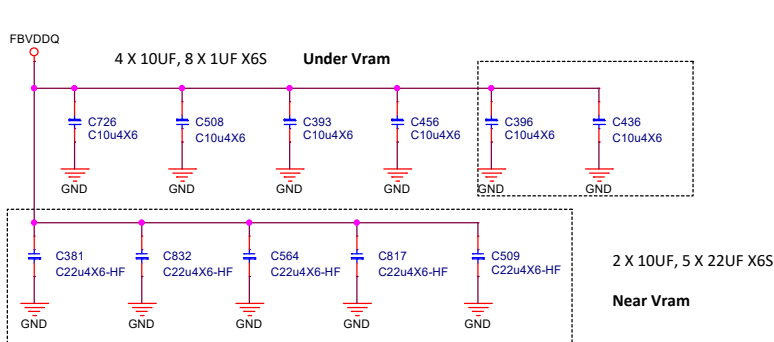
K4G80325FB-HC25-HF



K4G80325FB-HC25-HF

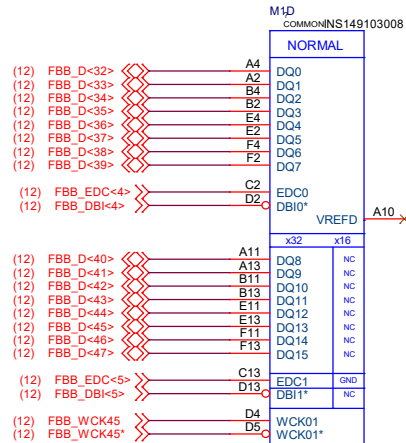


K4G80325FB-HC25-HF

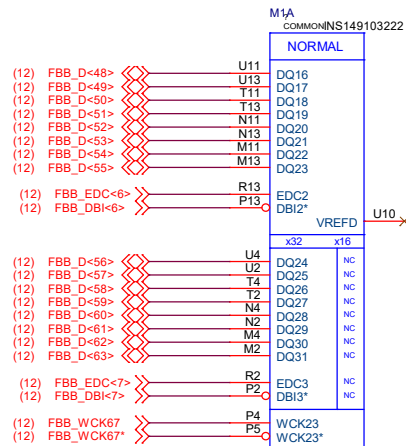




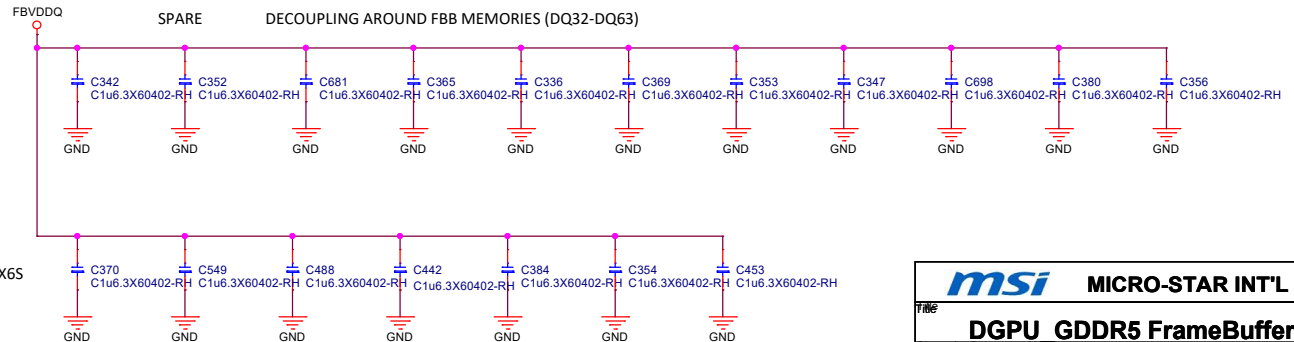
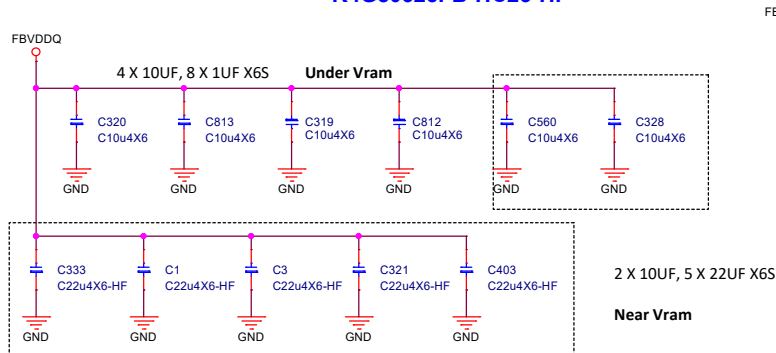
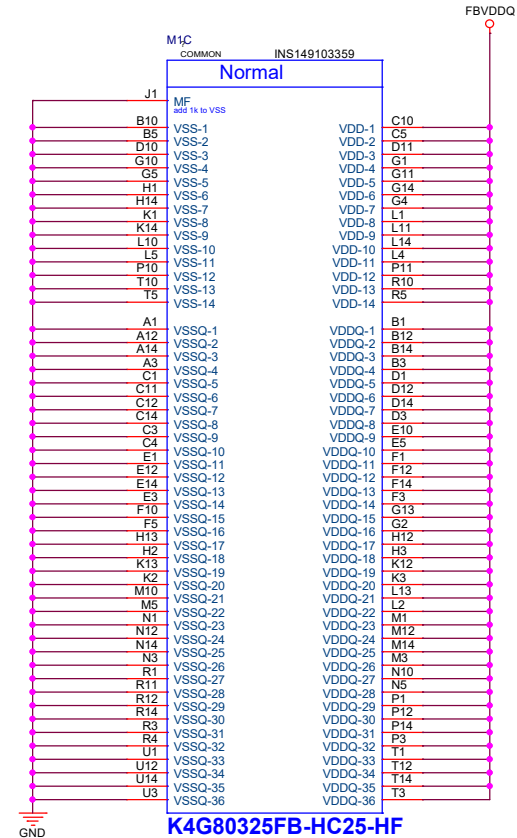
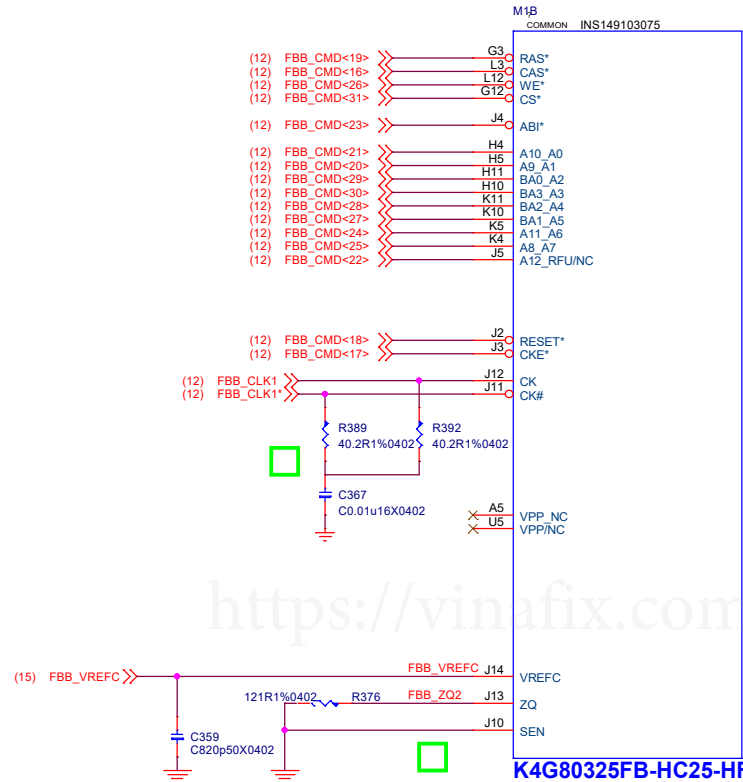
# DGPU\_GDDR5 FrameBuffer B1



K4G80325FB-HC25-HF

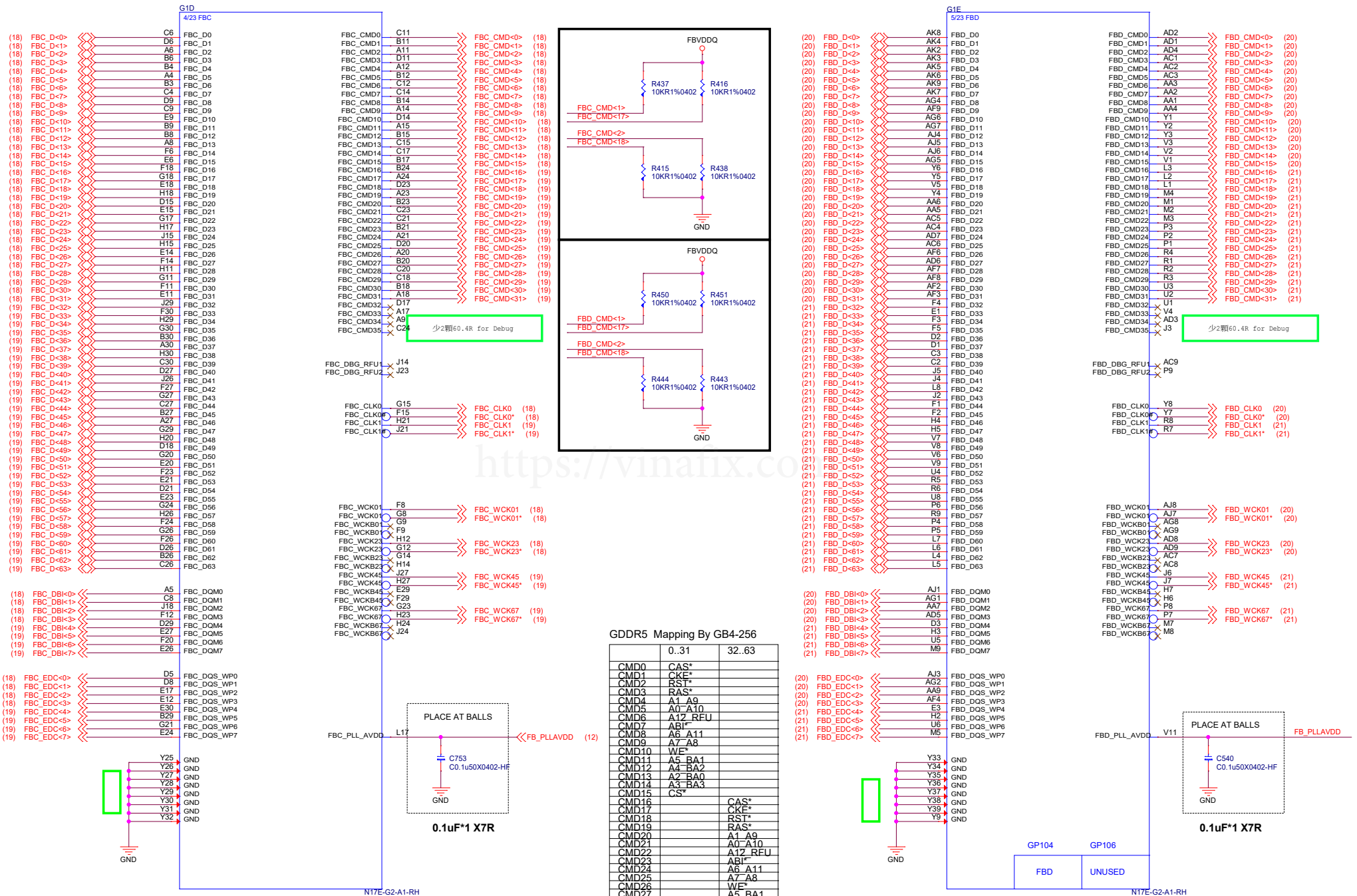


K4G80325FB-HC25-HF



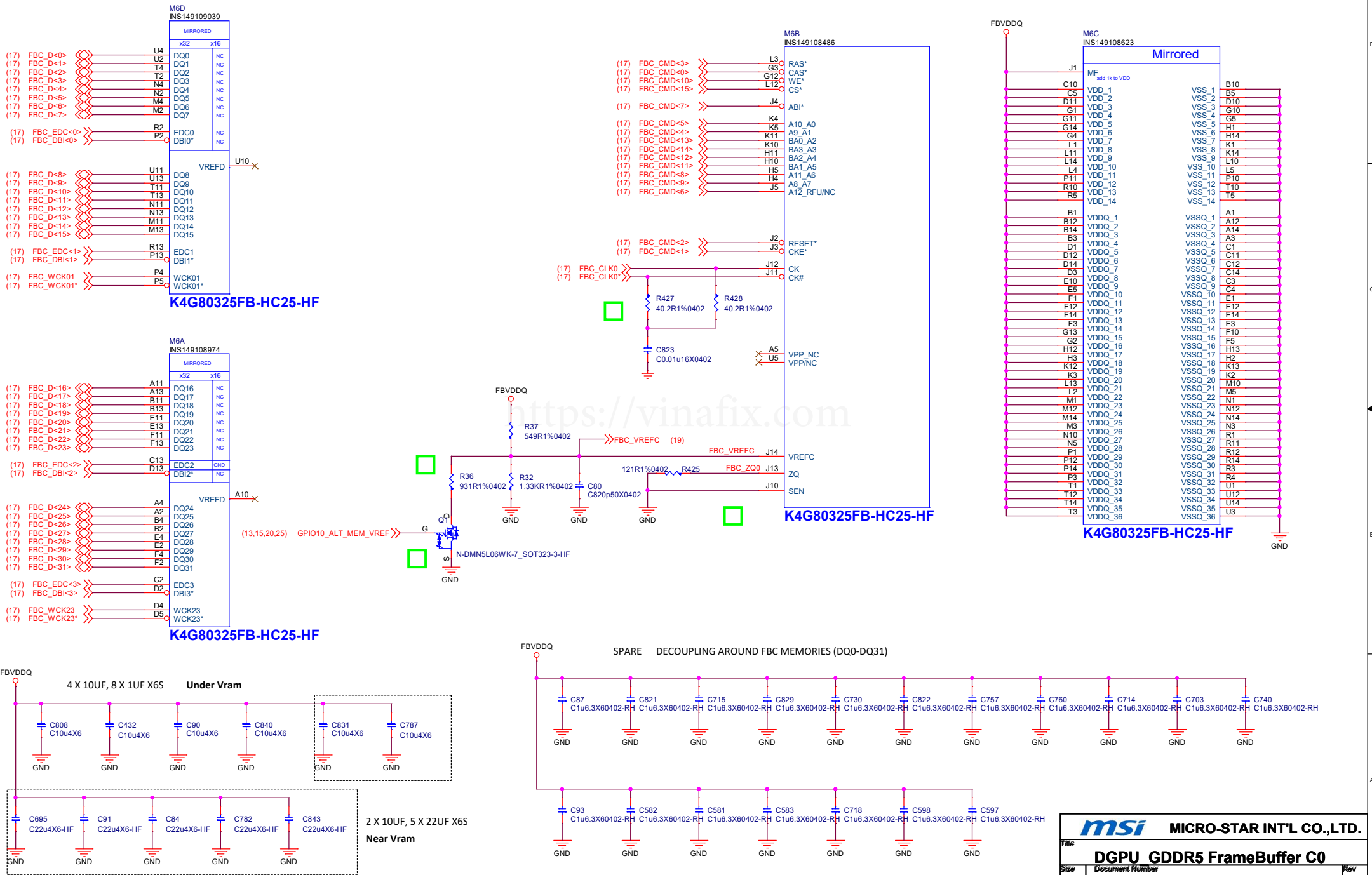


# GPU Frame Buffer Partition C/D



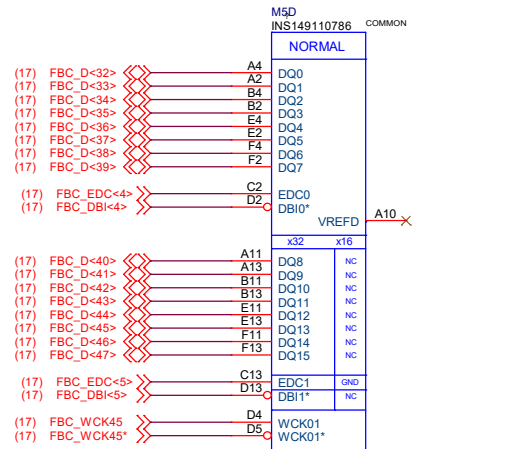


# DGPU\_GDDR5 FrameBuffer C0

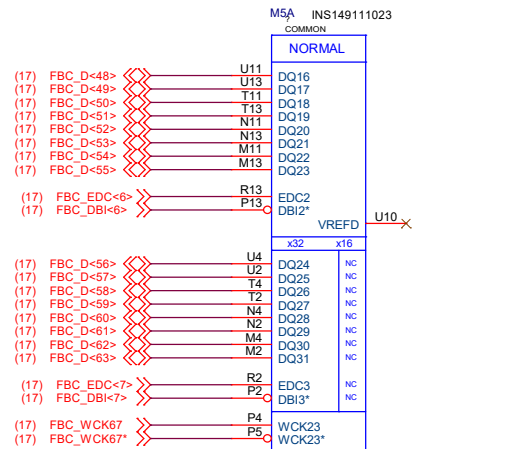




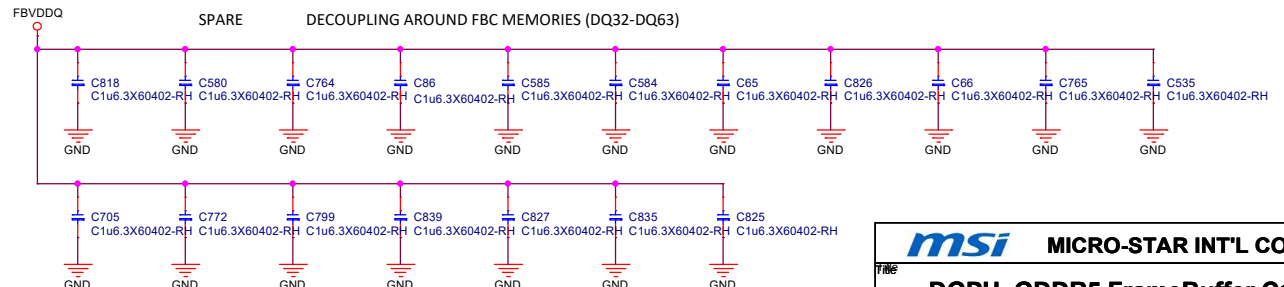
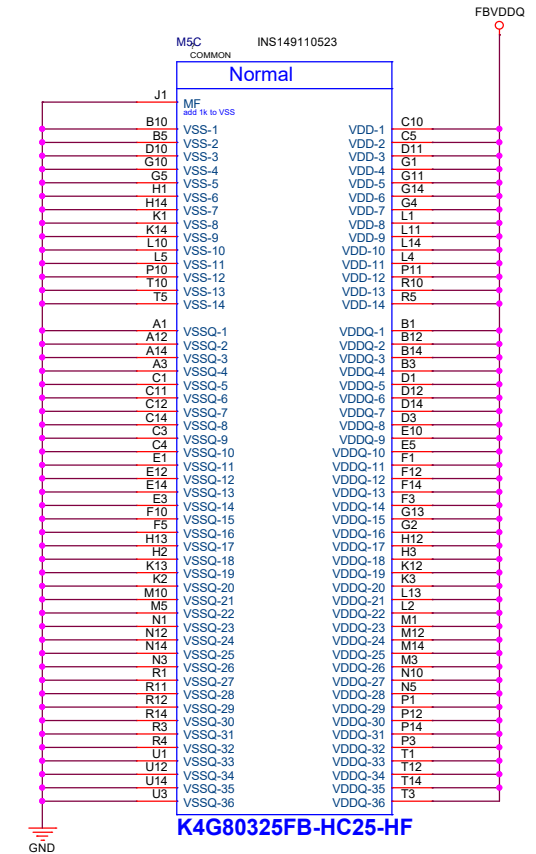
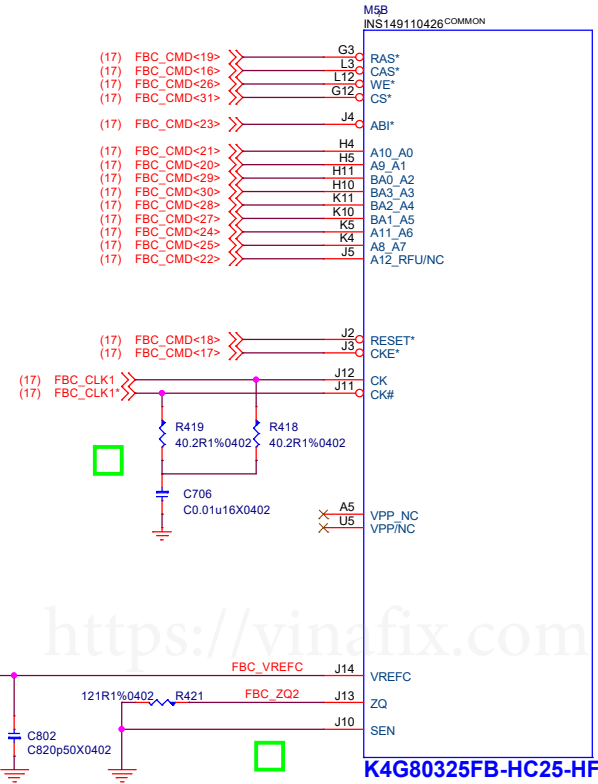
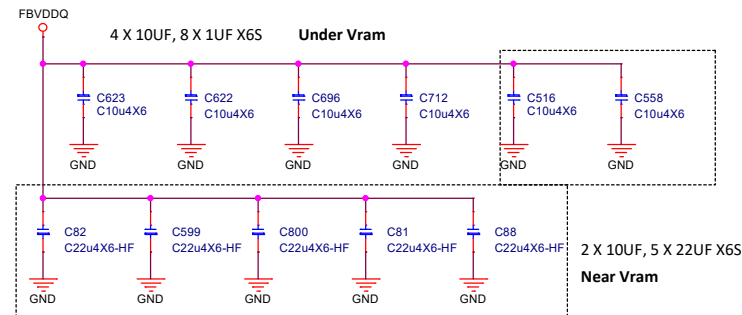
# DGPU\_GDDR5 FrameBuffer C1



K4G80325FB-HC25-HF

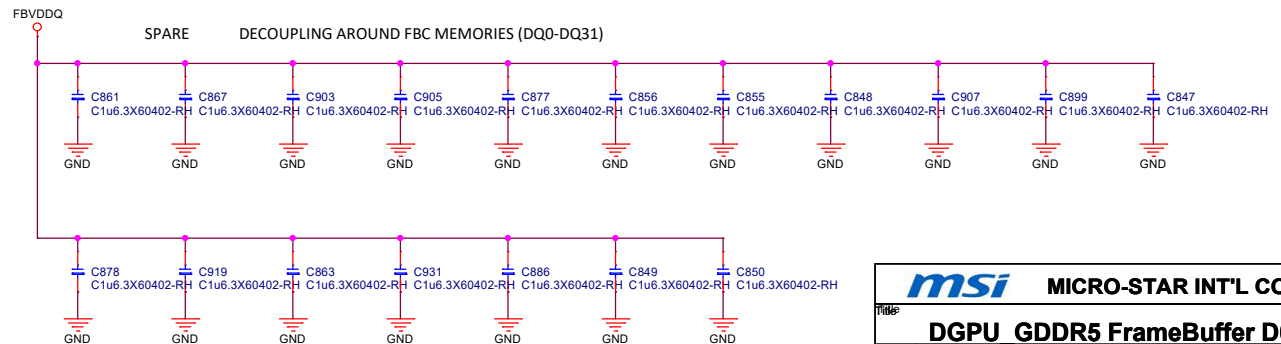
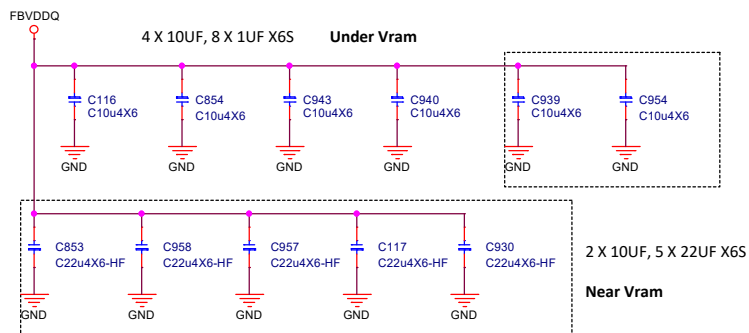
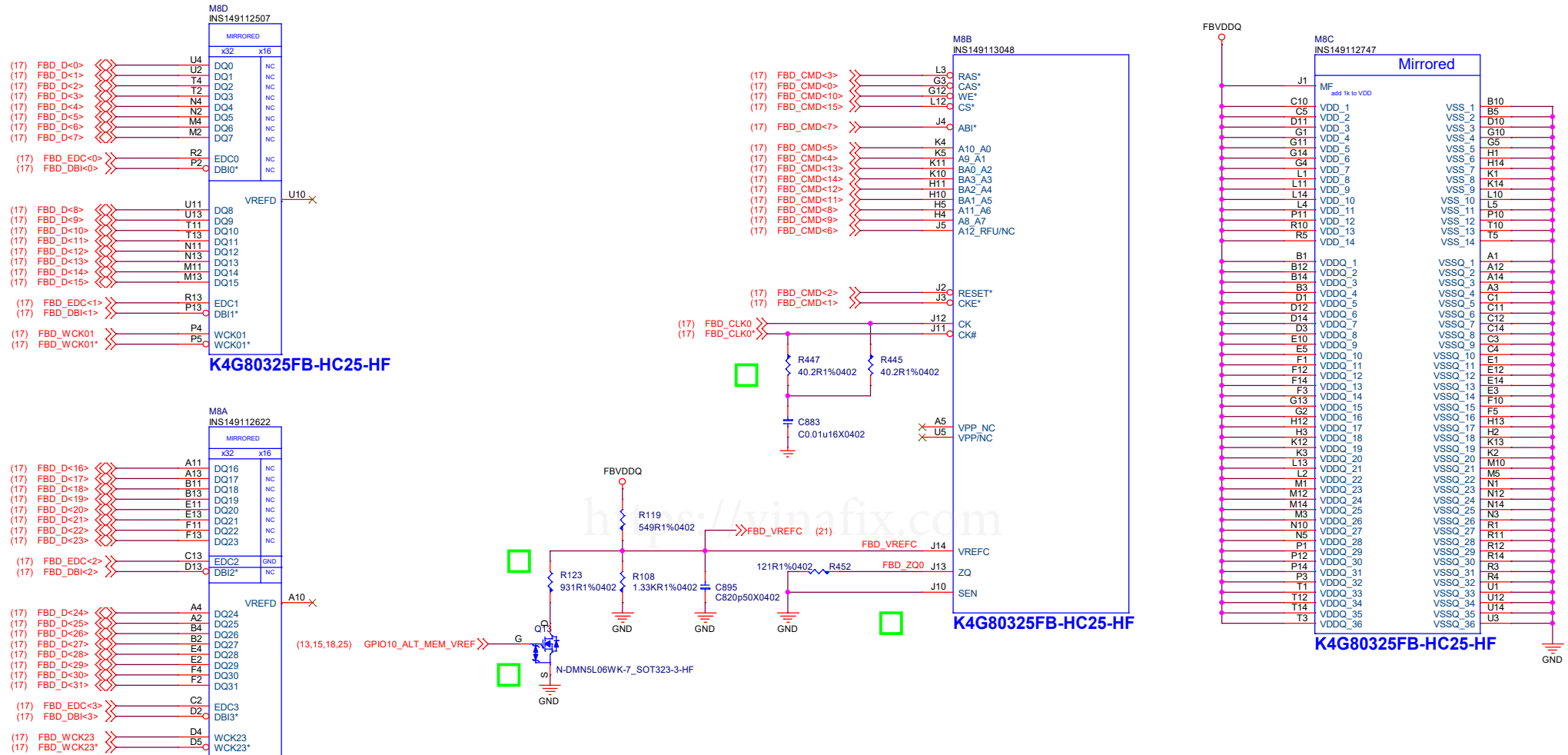


K4G80325FB-HC25-HF



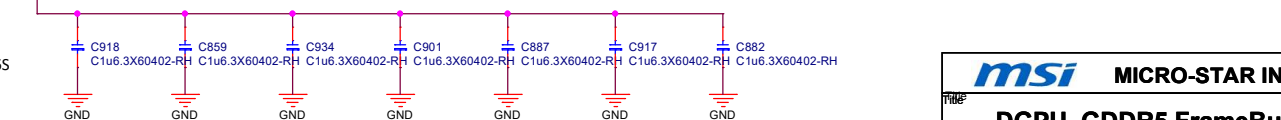
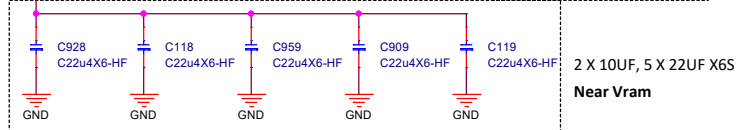
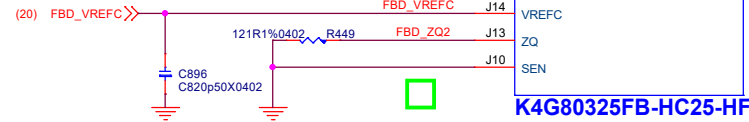
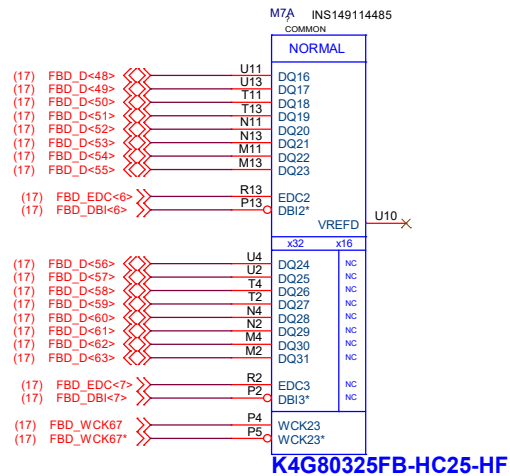


# DGPU\_GDDR5 FrameBuffer D0



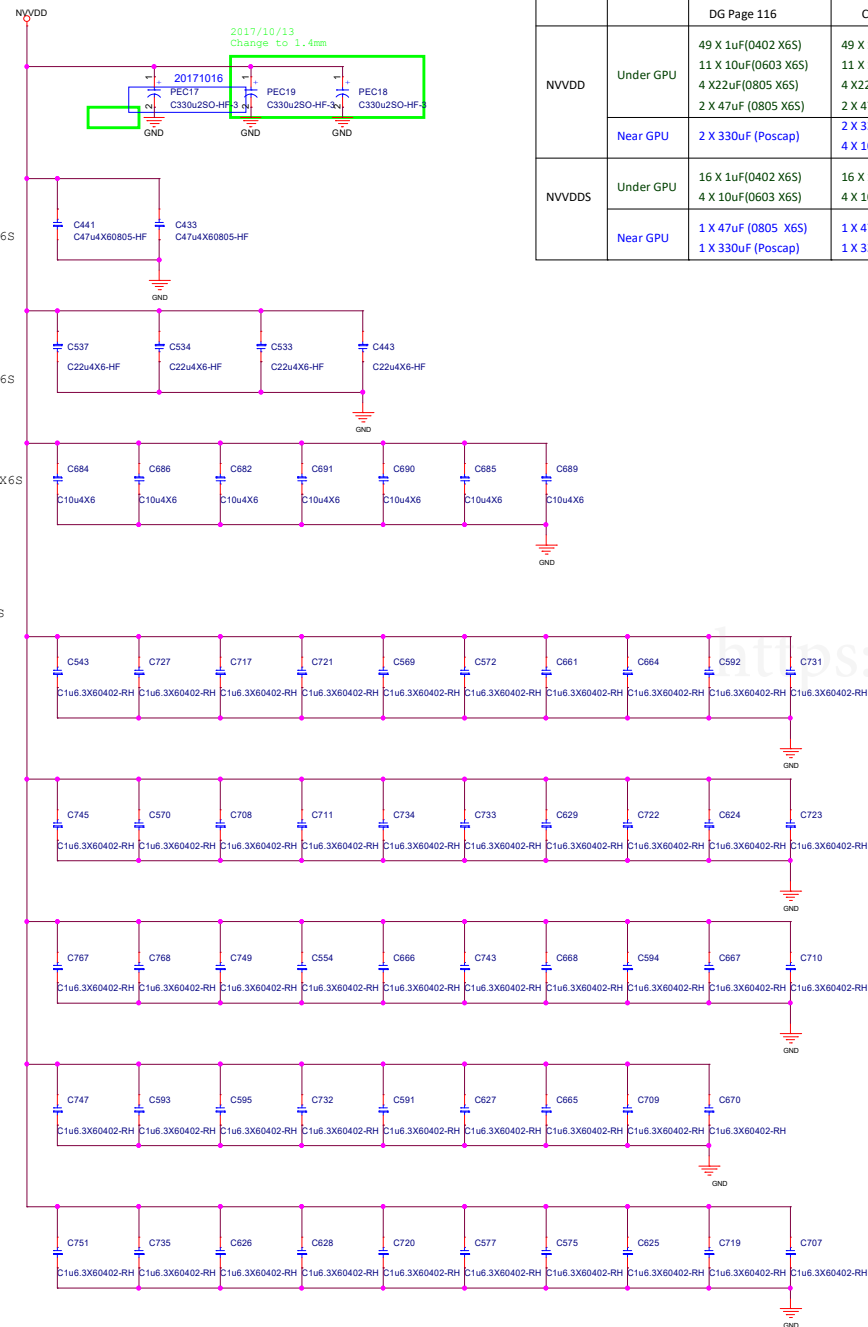


<https://vinafix.com>



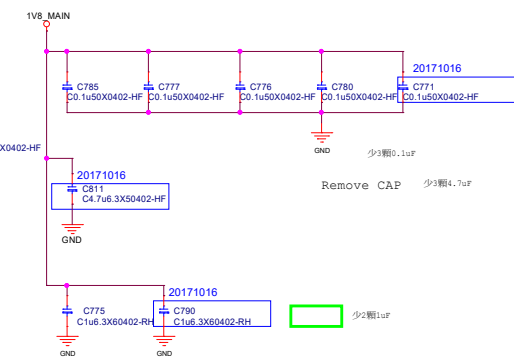
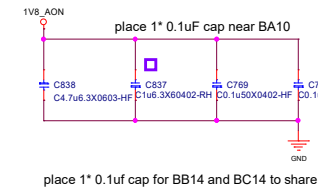
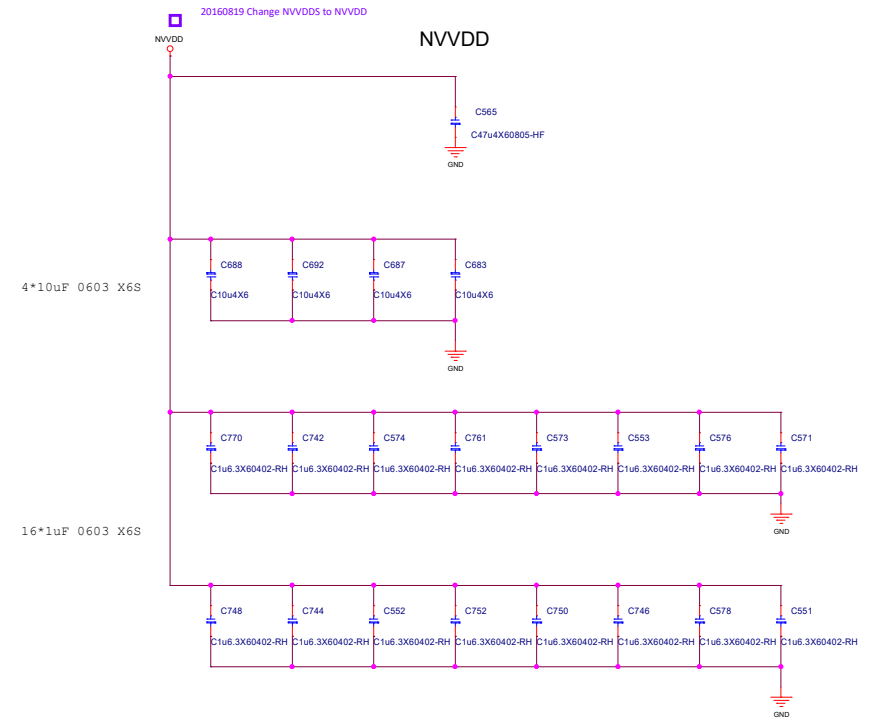


## NVVDD



		DG Page 116	CRB
NVVDD	Under GPU	49 X 1uF(0402 X6S) 11 X 10uF(0603 X6S) 4 X22uF(0805 X6S) 2 X 47uF (0805 X6S)	49 X 1uF(X7R 6.3V) 11 X 10uF(X6S 6.3V) 4 X22uF(X6S 6.3V) 2 X 47uF (X6S 4V)
	Near GPU	2 X 330uF (Poscap)	2 X 330uF (Poscap) 4 X 100uF (X5R 4V) ad
NVVDDS	Under GPU	16 X 1uF(0402 X6S) 4 X 10uF(0603 X6S)	16 X 1uF(X6S 6.3V) 4 X 10uF( 0603 X6S 4V)
	Near GPU	1 X 47uF (0805 X6S) 1 X 330uF (Poscap)	1 X 47uF (0805 X5R 4V) 1 X 330uF (AL-Polymer

## NVVDD

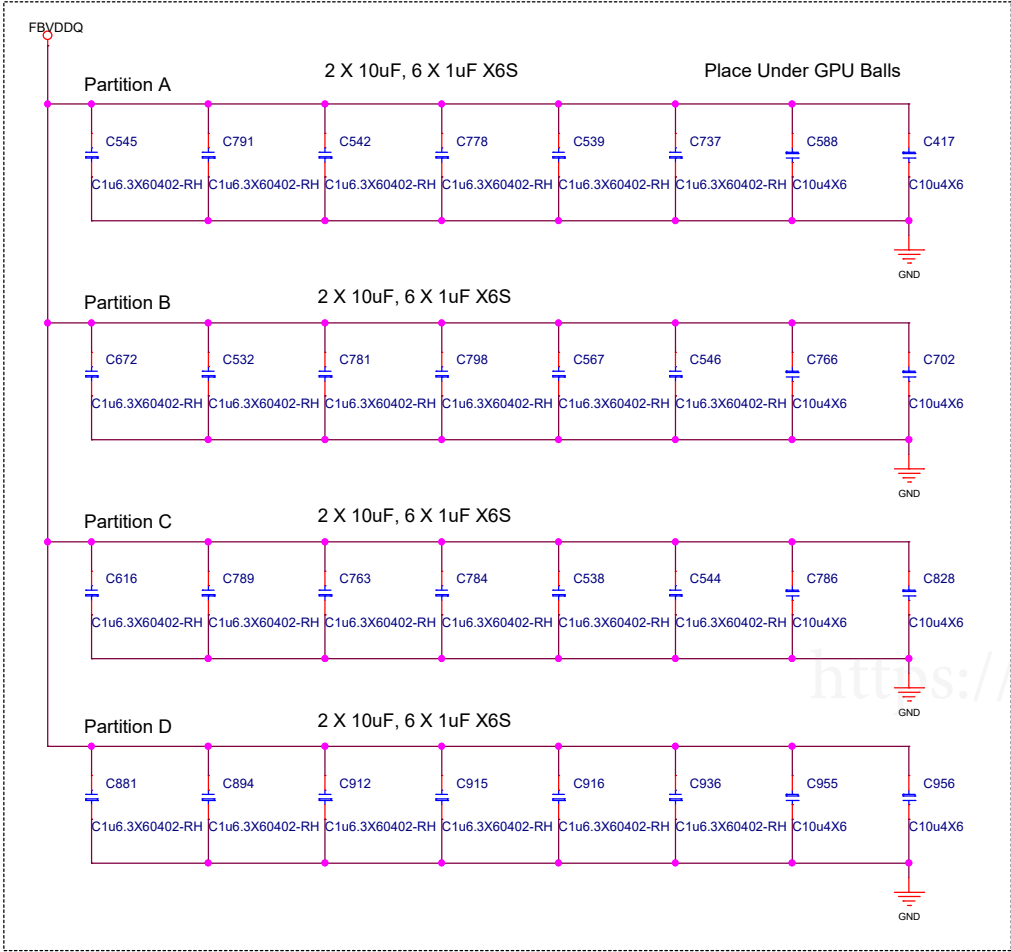


		DG Page 117	CRB
1V8_MAIN	Under GPU	7 X 0.1uF (0402)	7 X 0.1uF (0402 X7R)
	Near GPU	3 X 1uF (0402) 3 X 4.7uF (0603)	3 X 1uF (0603 X7R) 3 X 4.7uF (0603 X6S)
1V8_AON	Under GPU	2 X 0.1uF (0402)	2 X 0.1uF (0402 X7R)
	Near GPU	1 X 1uF (0402) 1 X 4.7uF (0603)	1 X 1uF (0603 X7R) 1 X 4.7uF (0603 X6S)

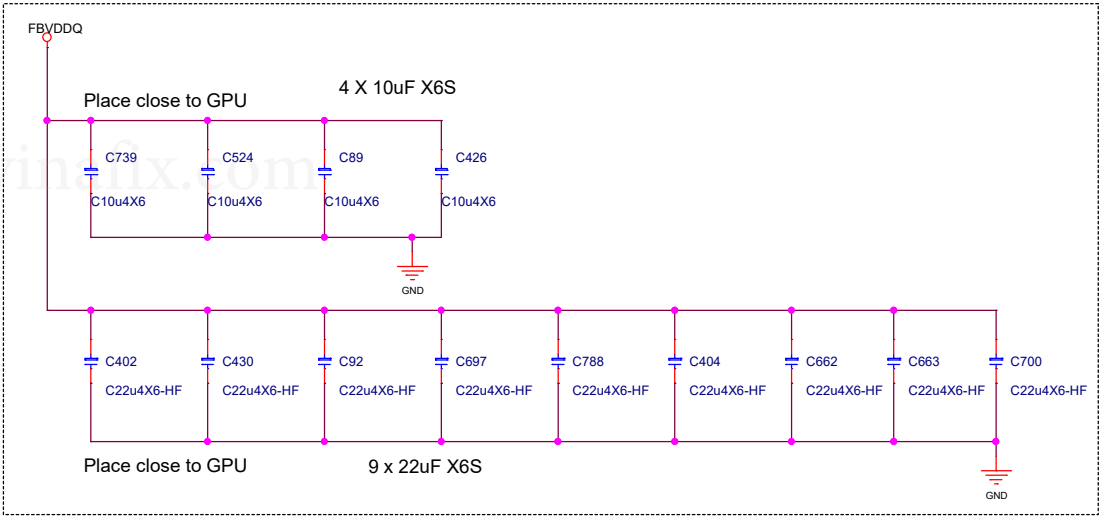


FBVDDQ

GPU DECOUPLING B



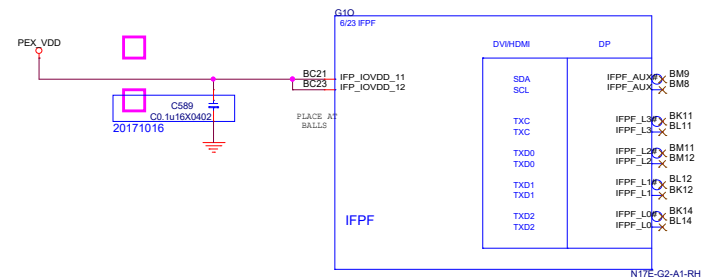
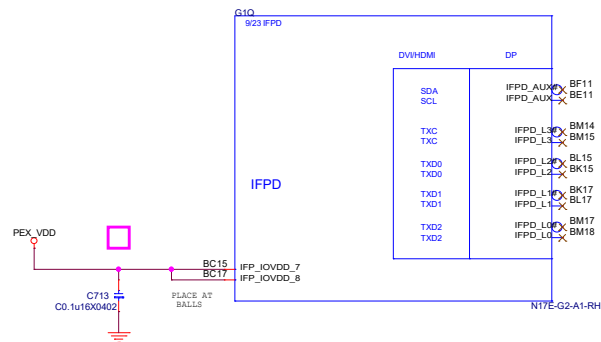
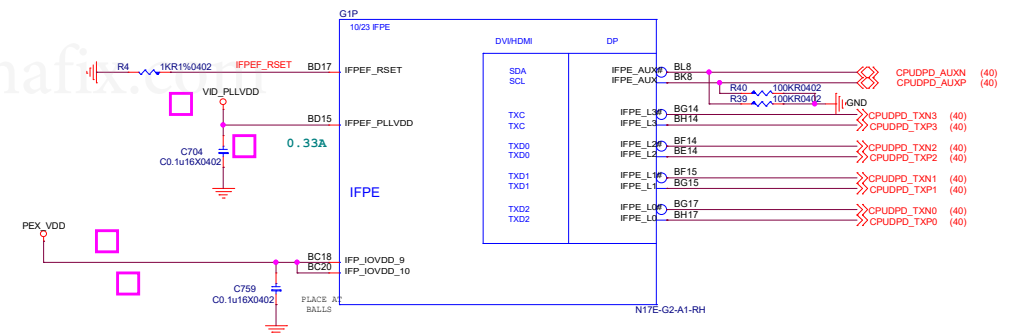
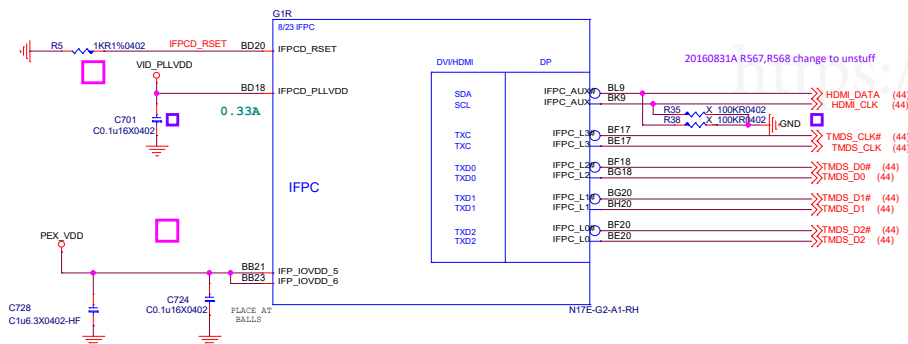
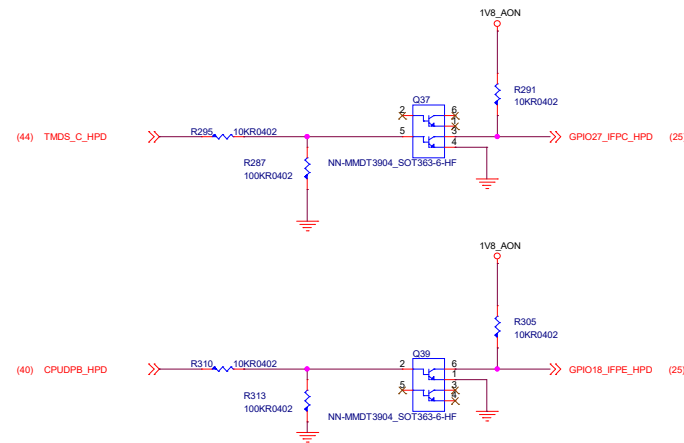
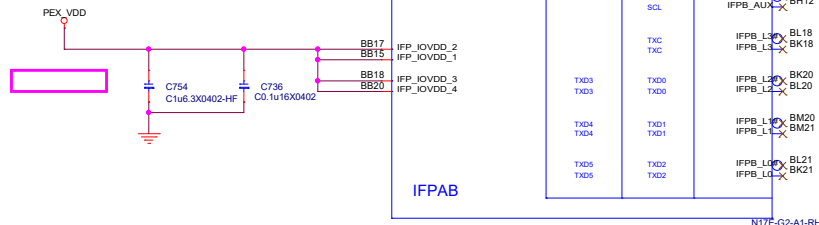
		DG Page 116	CRB
FBVDDQ (GPU side)	Under	24 X 1uF(0402 X6S) 5 X 10uF(0603 X6S)	24 X 1UF(0402 X6S 6.3V) 5 X 10uF(X6S 4V)
	Near	7 X 10uF(0603 X6S) 9 X 22uF(0603 X6S)	7 X 10uF(0603 X6S 4V) 9 X 22UF(0603 X6S 4V)





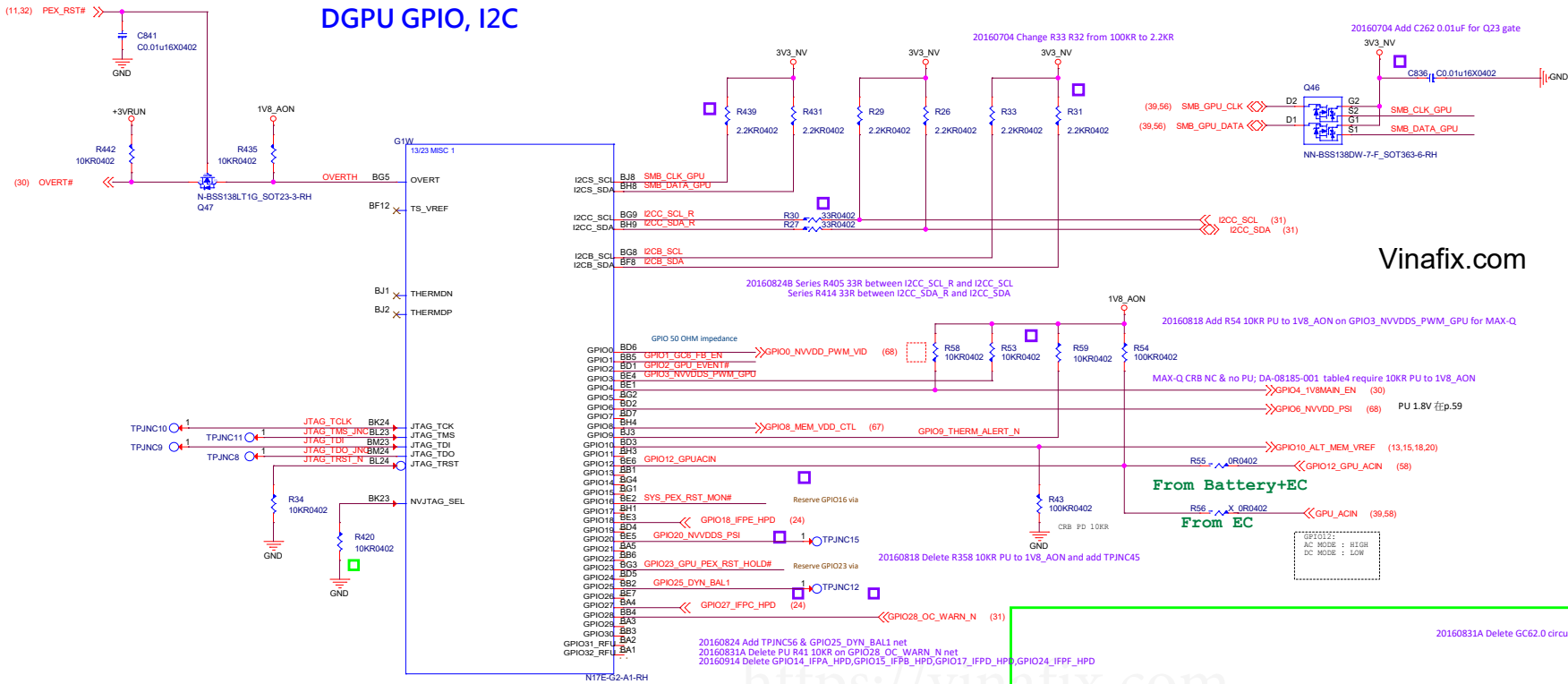
DG Page 117	Under GPU	Near GPU
IFP_IOVDD	12 X 0.1uF(0402 X6S)	3 X 4.7uF (0603) 3 X 1uF (0402)

0.305A for each IFP\_IOVDD in use



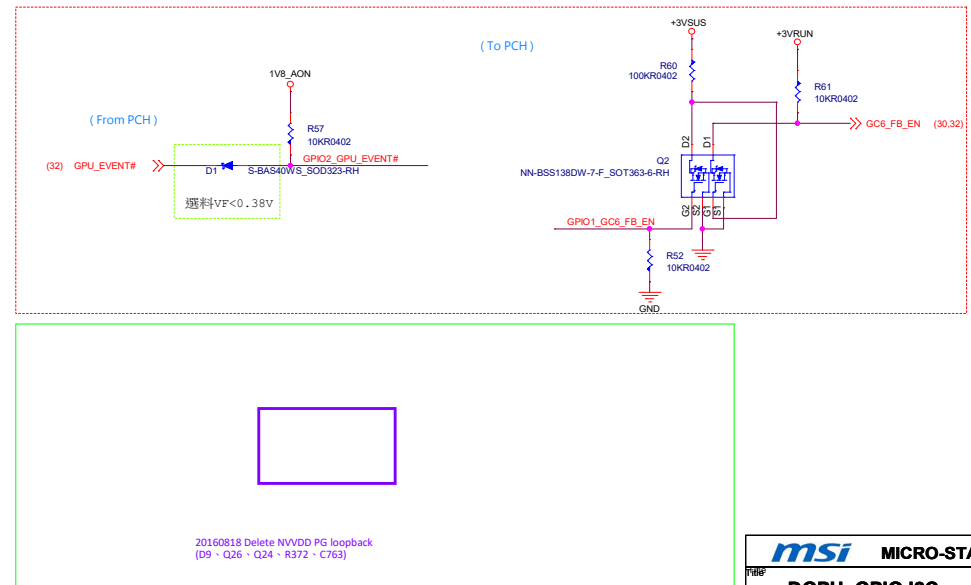


# DGPU GPIO, I2C



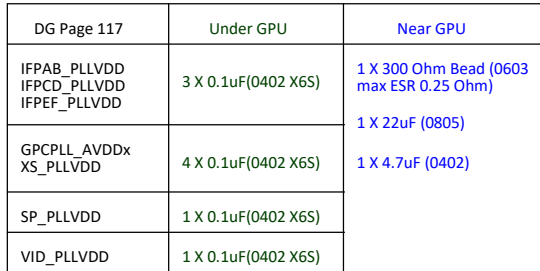
Vinafix.com

Pin Number	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to 1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source, 10K pull-down
GPIO2	GC6M: GPU_EVENT#/WAKE#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8_AON
GPIO3	NVVDD_PWM	O	PWM output to control the NVVDD power supply	0 to 1V8 output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8_AON
GPIO5	FRM_LCK#	I	Active low Fram Lock	OD, 10K pull-up to 1V8_AON
GPIO6	NVVDD_PSI#/NVVDD_PSI#	O	Phase shedding	10K pull-up to 1V8_AON
GPIO7	LCD_BL_PWM	O	Panel Backlight enable control signal to turn on a logo LED	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT#	I/O	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VDD; Quadro: Power_Brake#	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	
GPIO14	HPD_IFPA#	I	Hot Plug Detect for IFPA	Inverted input
GPIO15	HPD_IFPB#	I	Hot Plug Detect for IFPB	Inverted input
GPIO16	GC6M: SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 1V8_AON
GPIO17	HPD_IFPD#	I	Hot Plug Detect for IFPD	Inverted input
GPIO18	HPD_IFPE#	I	Hot Plug Detect for IFPE	Inverted input
GPIO19	3Dvision/STEREO	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE	I/O		
GPIO21	RASTER_SYNC0	I/O	Input when master GPU or Output when Slave GPU	100K pull-down
GPIO22	SWAP_RDY0 or SWAPRDY_IN	I/O	SLI Swap Ready Out	
GPIO23	GC6M: GPU_PEX_RST_HOLD#	I/O	GPU PCIe self-reset control	OD, 10K pull-up to gated 3V3
GPIO24	HPD_IFPF#	I	Hot Plug Detect for IFPF	Inverted input
GPIO25	Unused	I/O		
GPIO26	Unused	I/O		
GPIO27	HPD_IFPC#	I	Hot Plug Detect for IFPC	Inverted input
GPIO28	OC_WARN/HT	I	Over current throttling trigger	10K pull-up to 1V8_AON
GPIO29	EDPc_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	Unused	I/O		





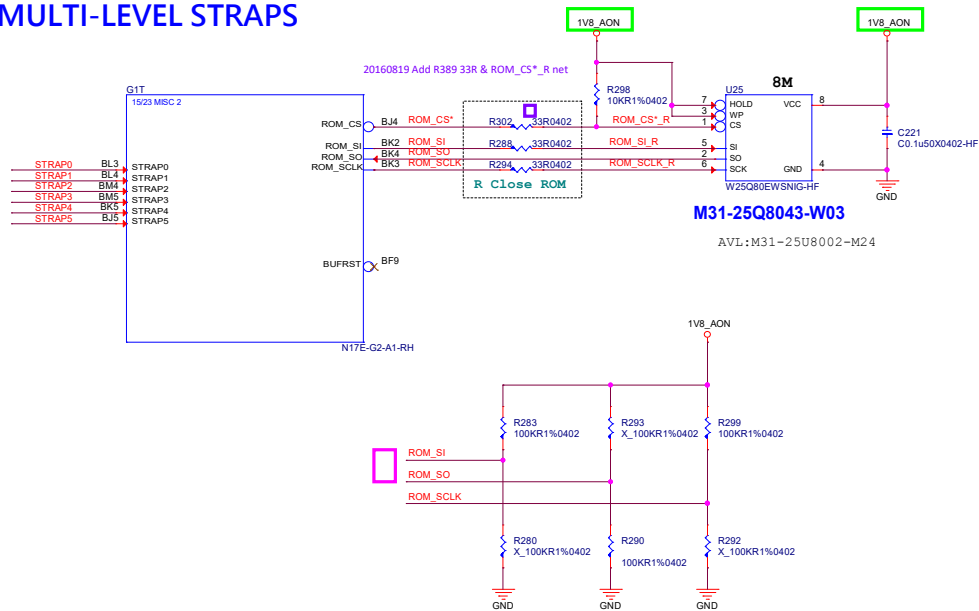
20160704 Add C1041 22uF & C1038 4.7uF & C1040 0.1uF for VID\_PLLVDD  
20160912A Delete C1041 & C1038



The diagram shows two blocks, MI0A and MI0B, with their respective inputs and outputs. The MI0A block (left) has inputs AM5, AM6, AM7, and AM9. The MI0B block (right) has inputs AV7, AV8, AV9, and AV11. Both blocks have multiple outputs labeled with AT, AV, and AB. The MI0A block is connected to a 1K1%0402 resistor R50 and a 1N7E-G2-A1-RH diode. The MI0B block is connected to a 1K1%0402 resistor R51 and a 1N7E-G2-A1-RH diode.



# ROM, MULTI-LEVEL STRAPS



STRAP2	STRAP1	STRAP0	RAMCFG[2:0]	
L	L	L	00000	V
L	L	H	00001	V
L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

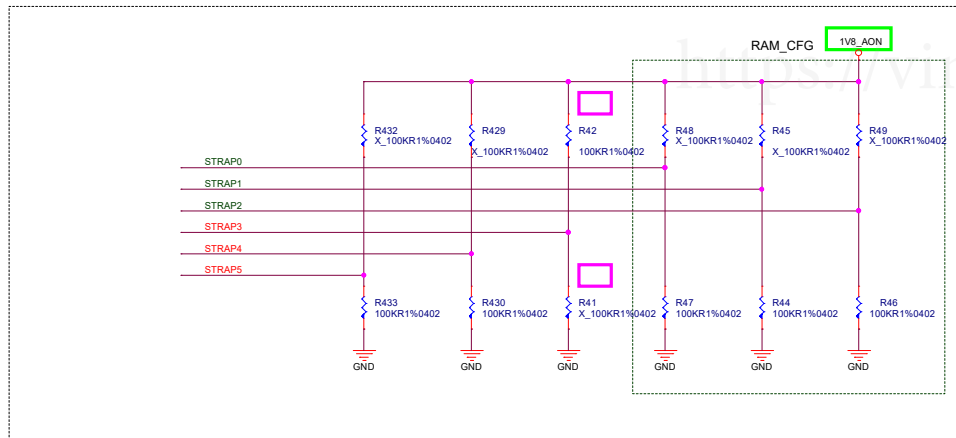
256M\*32  
SAMSUNG 0X0  
MICRON 0X1  
HYNIX 0X2

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	V
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

SOR\_EXPOSED :GPU AUDIO SETTING

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

1:SMB\_ALT\_ADDR ENABLE (DUAL GPU)  
0:SMB\_ALT\_ADDR DISABLE (SINGLE GPU)  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
1:PCIE\_CFG LOW SWING POWER  
0:PCIE\_CFG HIGH SWING POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

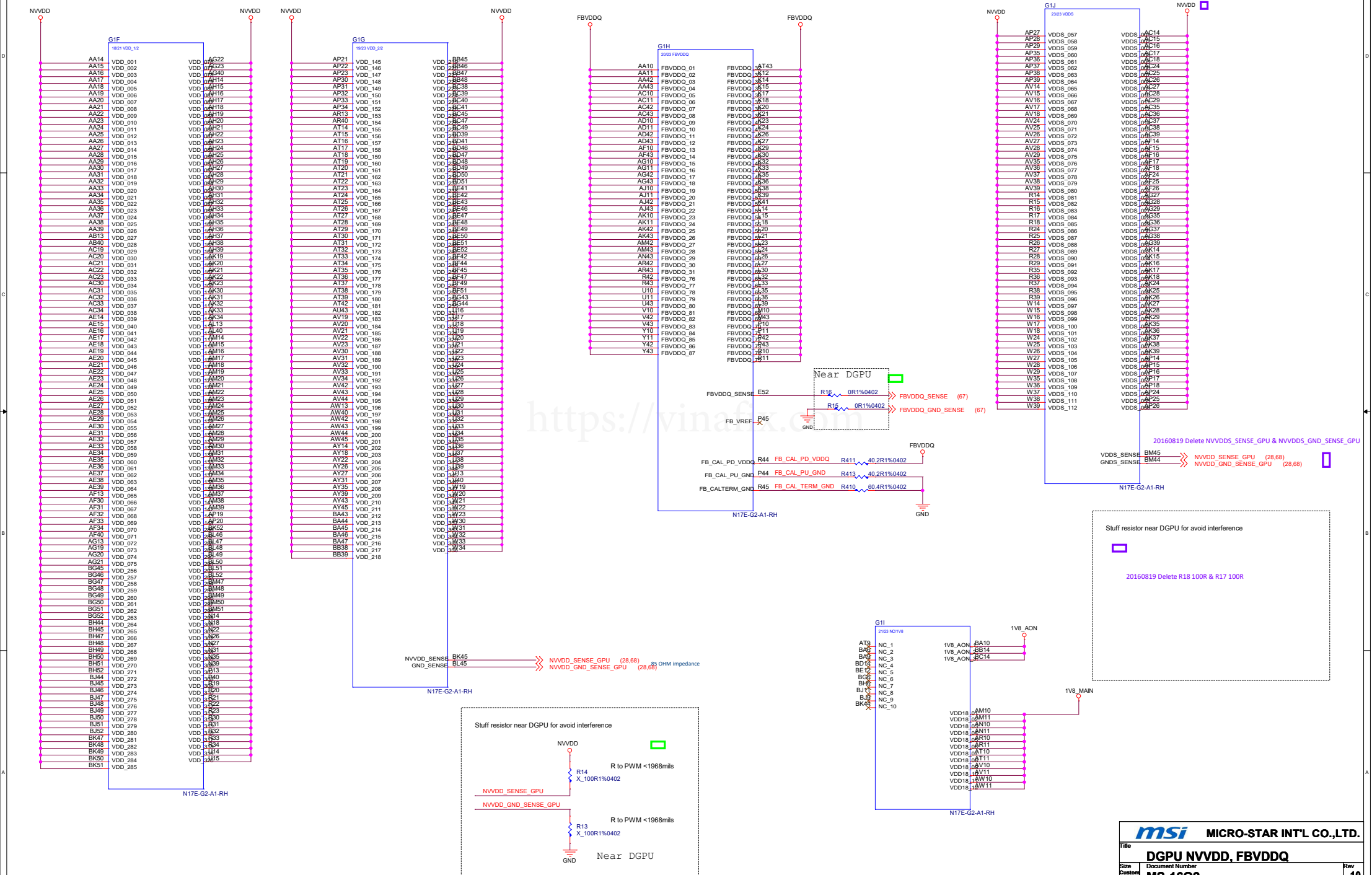


<p>V_TOP1</p> <p>5010</p> <p>256M*32</p> <p>DEFAULT SETTING</p> <p>SAMSUNG</p> <p>M12-8032535-S02</p> <p>X_K4G80325FB-HC25-HF</p>	
<p>V_TOP2</p> <p>5010</p> <p>256M*32</p> <p>MICRON</p> <p>M12-2563215-M30</p> <p>X_MT51J256M32HF-80-A-HF</p>	<p>20160817 Delete V_TOP3 M12-5GQ4H45-H23 and V_TOP4 M12-41325D5-502</p>



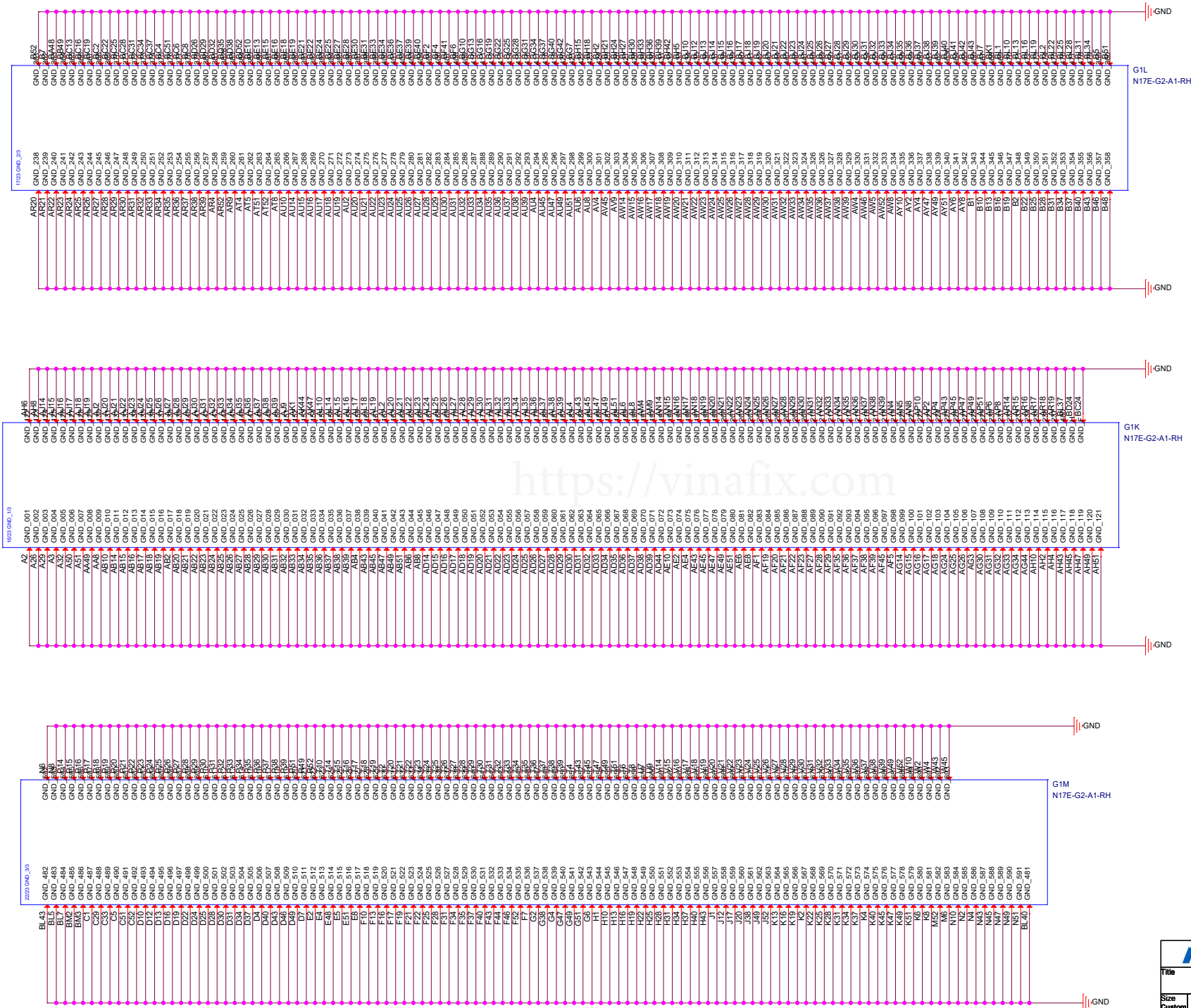
## GPU NVVDD, FBVDDQ

20160819 Change VDDS connect to NVVDD





DGPU GND



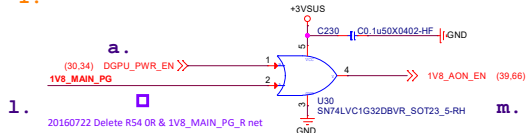


# nVIDIA Power Sequence Control

Power on = 1V8\_AON -> 1V8\_MAIN -> 3V3\_NV -> NVVDD -> PEX\_VDD -> FBVDDQ -> DGPUPWRGD

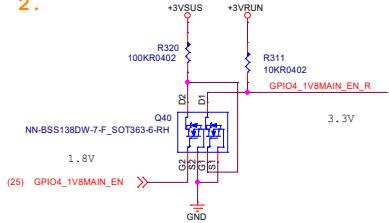
Power off = DGPUPWREN -> (PEX\_VDD -> NVVDDQ -> 3V3\_NV) -> FBVDDQ -> 1V8\_MAIN -> 1V8\_AON

1.

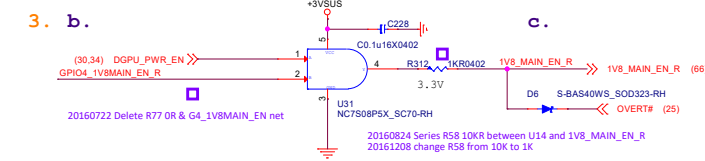


1.

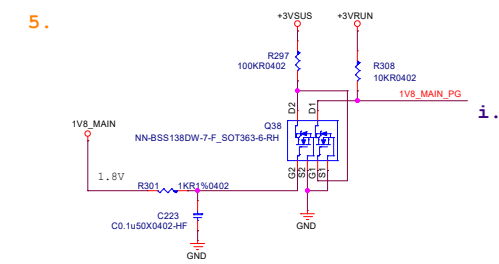
2.



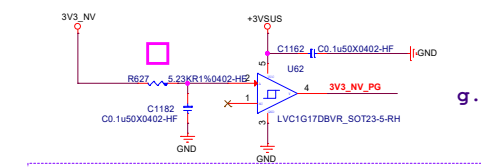
3.



5.



7.

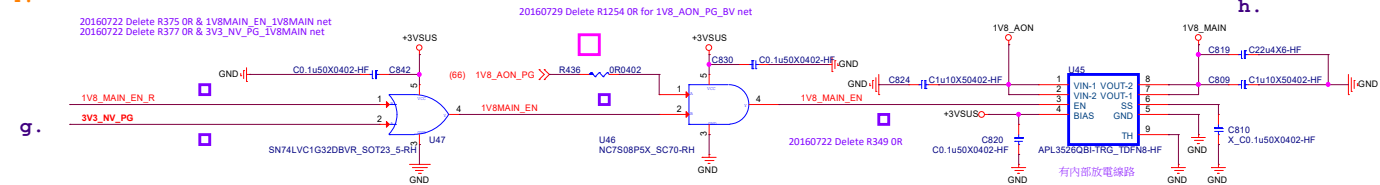


1V8\_AON Power Good By Voltage and delay

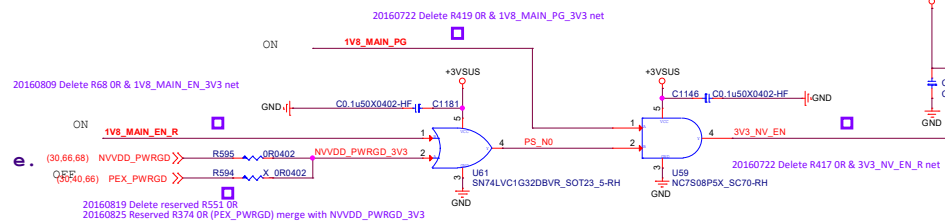
20160729 Delete U74 - C2892 - C8601 - R605 for 1V8\_AON\_PG\_BV ent

The ramp time for any rail must be more than 40us and is recommended to be less than 2ms  
From 1V8\_MAIN\_EN to PEX\_VDD must NOT exceed 4ms

4.



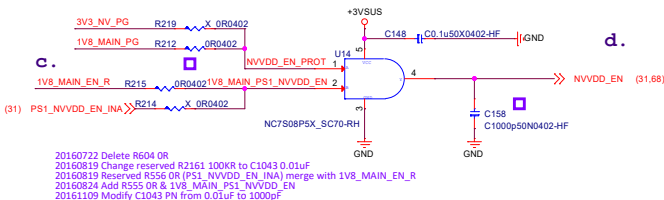
6.



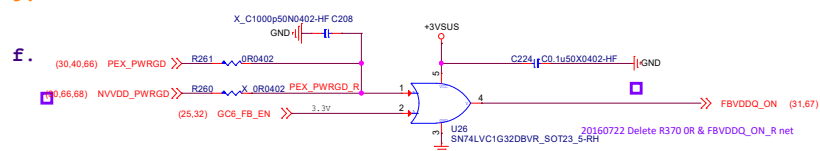
NVVDD Power Enable

The propagation delay between 1V8\_MAIN\_EN and the NVVDD\_EN needs to be less than 300us during both power up and power down

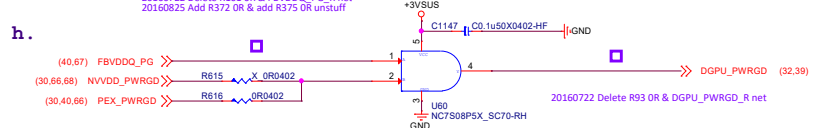
8.



9.

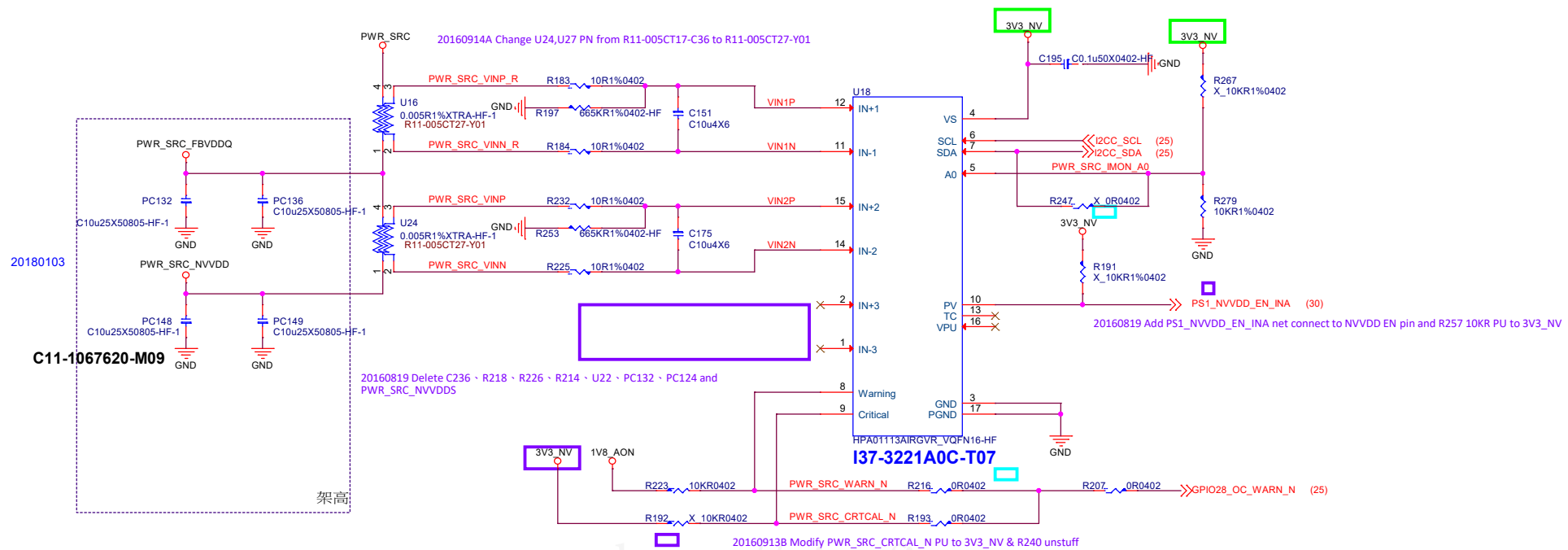


10.

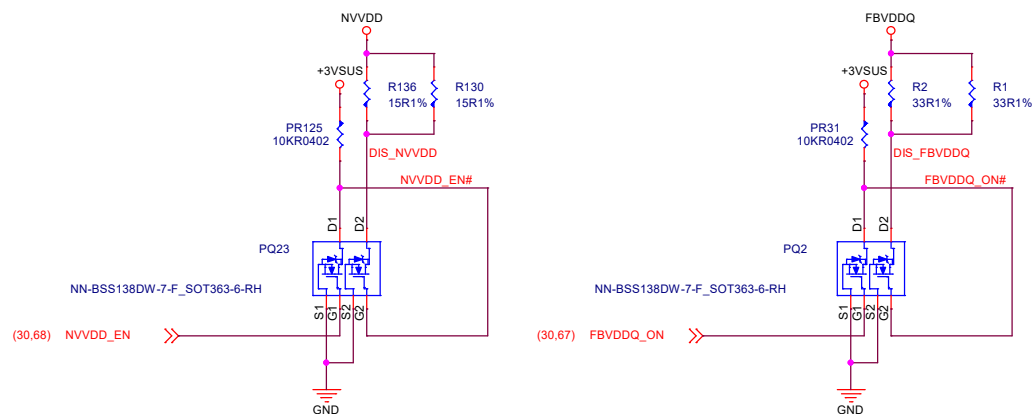




# DGPU\_Power Control



## Discharge



PEX\_VDD 内部放電4ms

3V3\_AON内部放電 2ms

1V8AON内部放電2ms

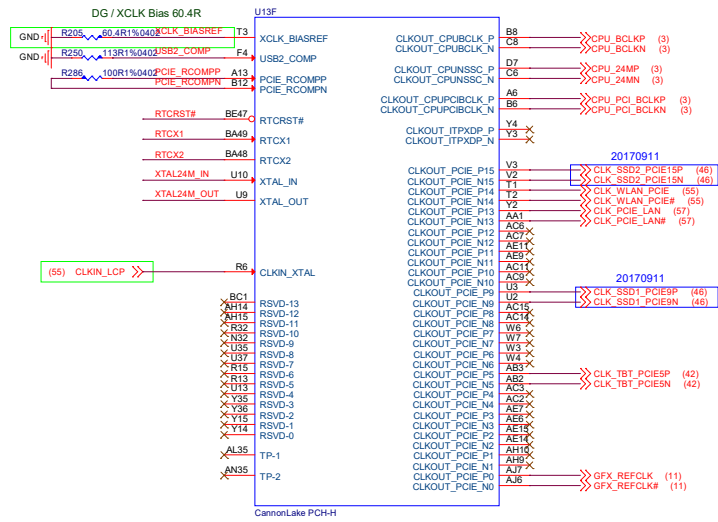
1V8\_MAIN内部放電320us

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msi MICRO-STAR INT'L CO.,LTD.	
File	DGPU Discharge
Size	Document Number
Custom	MS-16Q2
Date	Thursday, January 25, 2018
Sheet	31 of 73
Rev	10

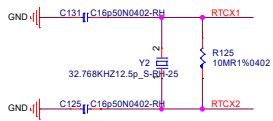


## HM370 (RTC/PCIE\_Clock/Clock/RSVD)



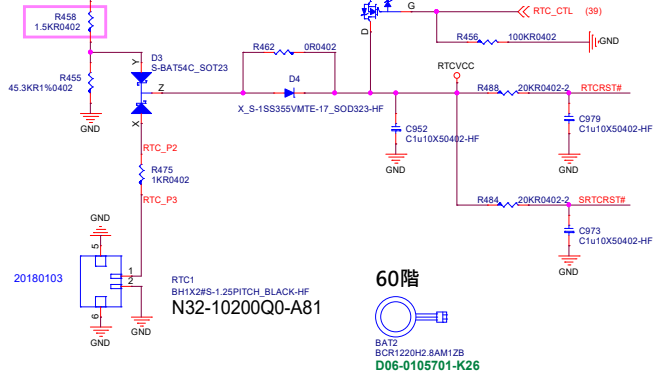
20170828 R2175 change to 200K  
to follow DG and CRB

### RTC Block(Close to PCH)

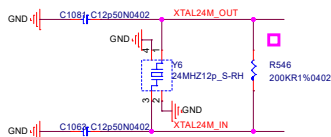


20170731 change R2185 to 1.5K to follow DG

**RTCVCC**



## 24MHz Clock

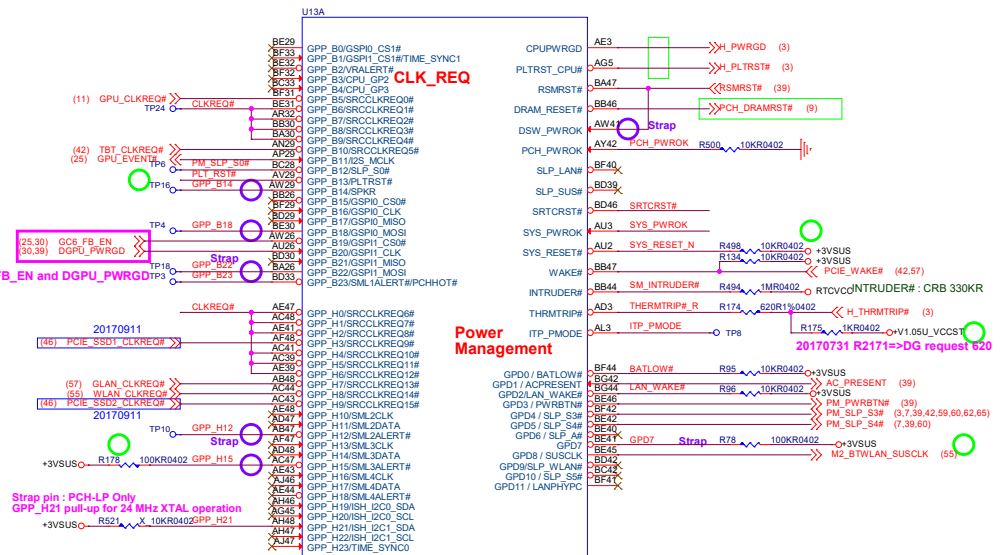


60階



BAT2  
BCR1220H2.8AM1ZB  
D06-0105701-K26

## HM370 (CLKREQ/ACPI)



### Functional Strap Definitions

## SPKR / GPP\_B14

The signal has a weak internal pull-down.  
0 = Disable Top Swap mode. (Default)

GSPI0\_MOSI / GPP\_B18

The signal has a weak internal pull-down.  
0 = Disable No Reboot mode. (Default)  
1 = Enable No Reboot mode.

CSPI1, MOSI / GPB\_B22

This Signal has a weak internal pull-down  
Bit 6 Boot BIOS Destination

Bit 0 Boot BIOS	Destination
0	SPI (Default)
1	LPB

SML1ALERT# / PCHHOT# / GPP

This signal has an internal pull-down.

GPR\_H12

**GFP\_H12**  
This signal has a weak

	This signal has a weak internal pull-down

## GPP\_H15

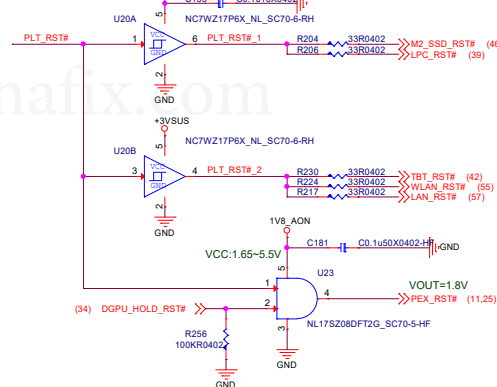
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

--	--

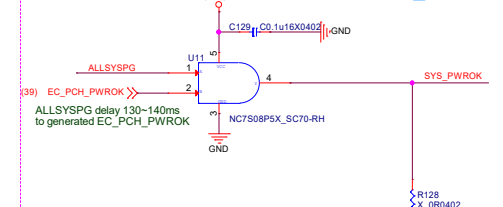
**GPPD7**  
External pull-up is required. Recommend 100K.  
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling


DG/ RTC Well Input Strap

PLT\_RST#



**SYS\_PWROK**



PCH\_PWROK



# HM370 (DMI/PCIE/USB3.1/USB2.0/CNVi)

Figure 14-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29		
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7	USB3.1 Gen1 #8	USB3.1 Gen1 #9	USB3.1 Gen1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	SATA 1a	SATA 1b	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4					GbE			GbE		GbE												
Intel® RST Support											No Support	No Support					Yes				No Support					Yes					Yes	

SKU	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1/Gen2 #7	USB3.1 Gen1/Gen2 #8	USB3.1 Gen1/Gen2 #9	USB3.1 Gen1/Gen2 #10	PCIe #5	PCIe #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	SATA 1a	SATA 1b	PCIe #13	PCIe #14	PCIe #15	PCIe #16	PCIe #17	PCIe #18	PCIe #19	PCIe #20	PCIe #21	PCIe #22	PCIe #23	PCIe #24
HM370	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	LAN Only	N/A	N/A	N/A	N/A	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN
QM370	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN
CM246	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	Gen1/Gen2	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN

- Added 4 new PCIe 3.0 lanes versus KBL-H platform.
- GbE LAN removed from lane 10 and SATA #0/#1 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

## PCIE 9-12(M2)

## USB 3.1 CNT-2

## USB 3.1 CNT-1

## USB 3.1 CNT-3

Ref DG Section 18.6  
- use Port 14 with CNVi Solution

## BT

## Webcam

## Fingerprint

## Multi-Color KB

## USB 3.1 CNT-2

## USB 3.1 CNT-3

## USB 3.1 CNT-1

## USB 2.0

## USB 3.1

## CNVi

CannonLake PCH-H

## USB 2.0

## CNVi

## USB 2.0

## CNVi

## USB 2.0

## CNVi

## USB 2.0

## CNVi

## USB 2.0

## CNVi

## USB 2.0

## CNVi

## USB 2.0

## CNVi

## USB 2.0

## CNVi

## USB 2.0

## CNVi

## USB 2.0

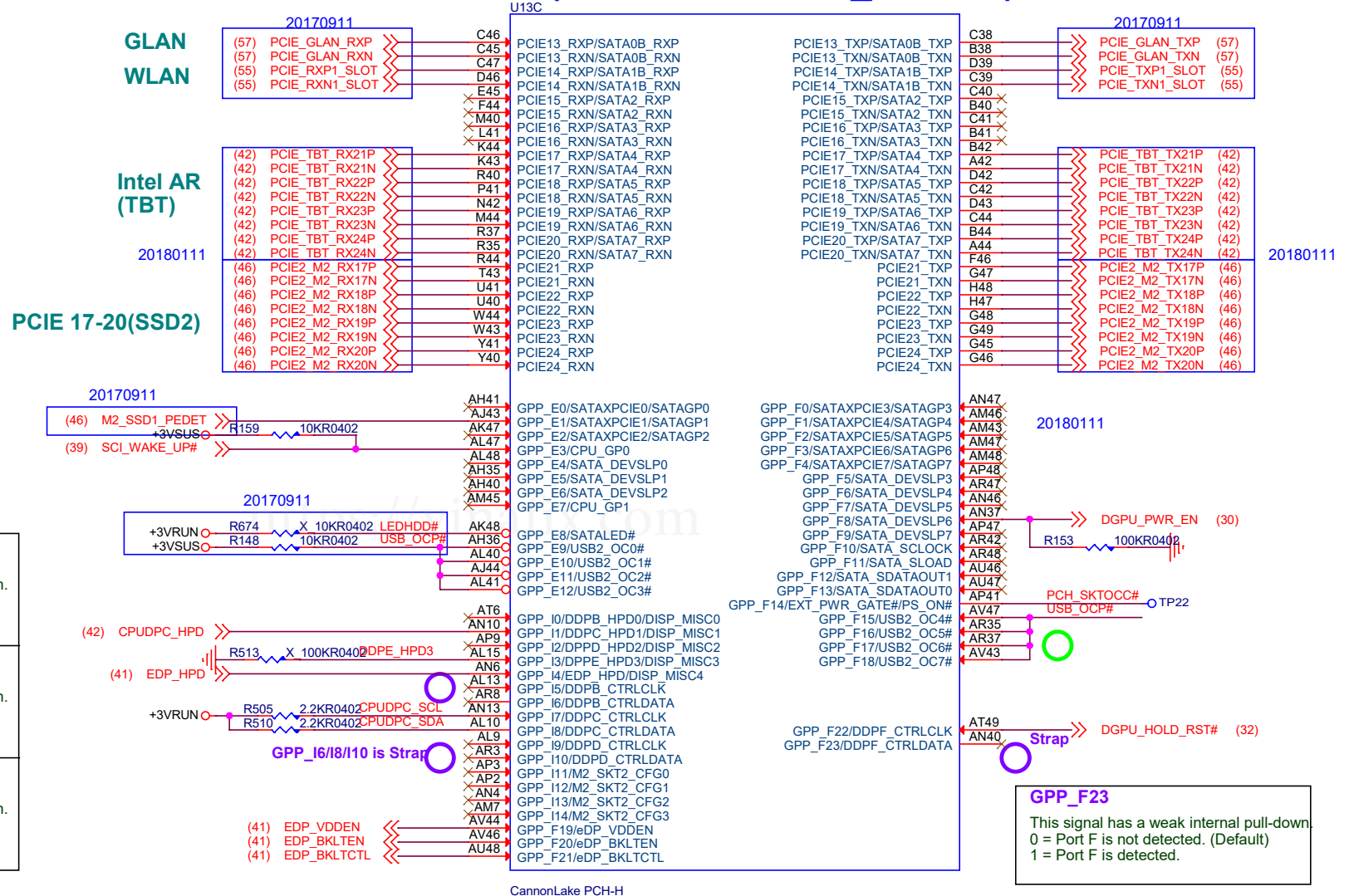
## CNVi

## USB 2.0

## CNVi



# HM370(SATA/PCIE/USB\_OC/DDI)



**msi**

**MICRO-STAR INT'L CO.,LTD.**

Title			<b>PCH-3(SATA/PCIE/USB_OC/DDI)</b>
Size	Document Number	Rev	
Custom	<b>MS-16Q2</b>	<b>10</b>	
Date:	Thursday, January 25, 2018	Sheet	34 of 73



# HM370 (HDA/GPIO/TJAG)

## Functional Strap Definitions

### SMBALERT# / GPP\_C2

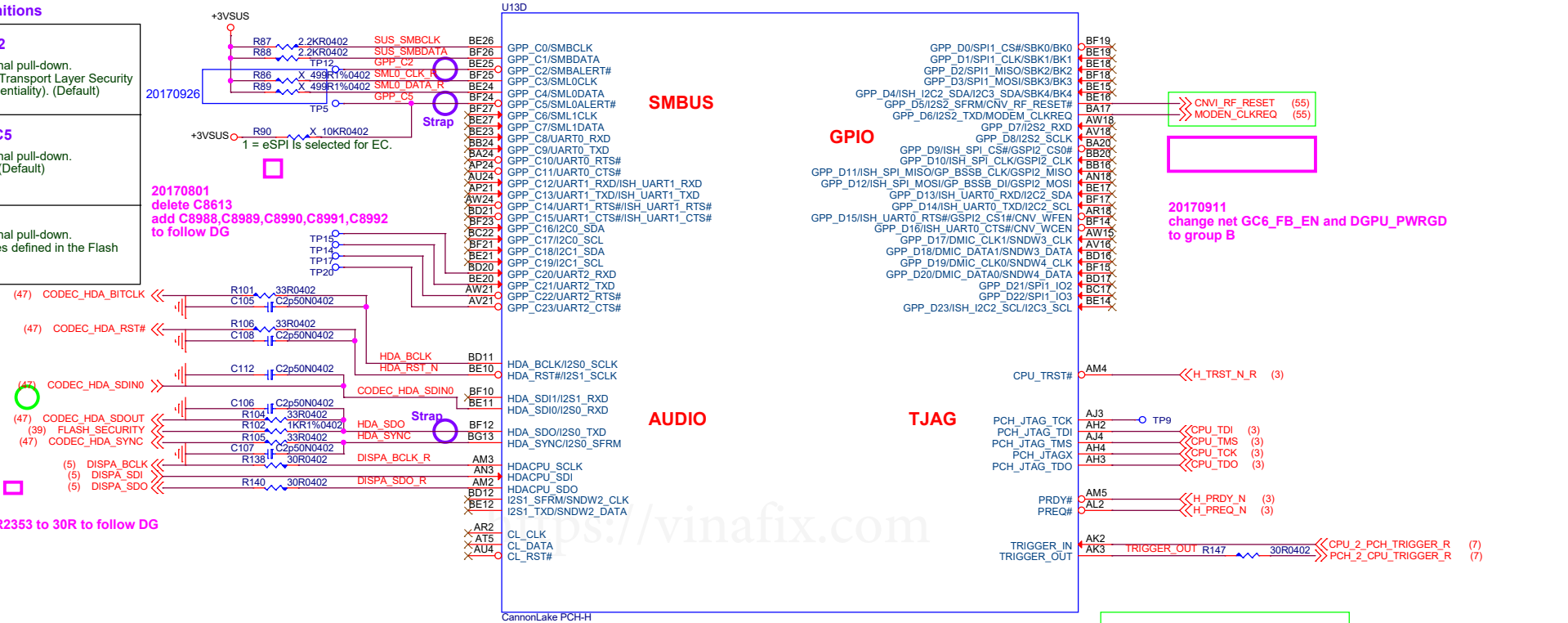
This signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

### SML0ALERT# / GPP\_C5

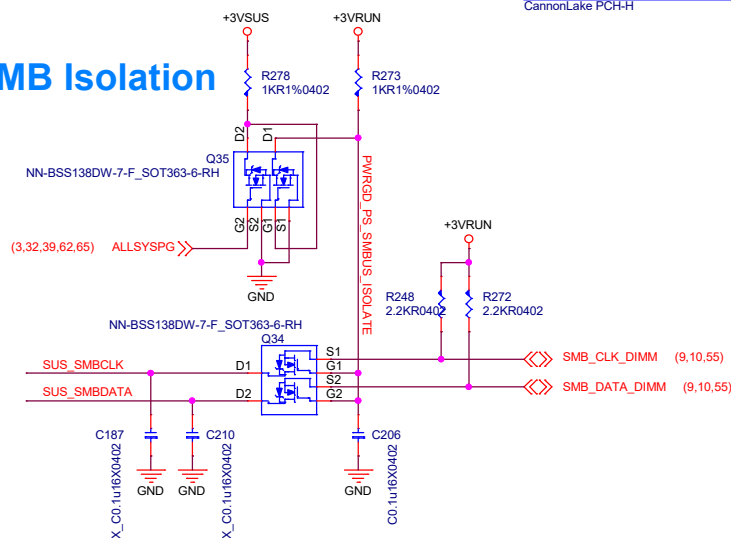
This signal has a weak internal pull-down.  
0 = LPC Is selected for EC. (Default)  
1 = eSPI Is selected for EC.

### HDA\_SDO

This signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor. (Default)



## SMB Isolation



ref DG / Chapter Platform and Test Hooks  
CPU\_TDO : PU 100R Near CPU (DG : R1)  
PU 100R Near PCH (DG : R3)  
CPU\_TDI : PU 51R Near PCH (DG : R4)  
CPU\_TMS : PU 51R Near PCH (DG : R5)  
CPU\_TCK : 51R to GND Near CPU (DG : R2)

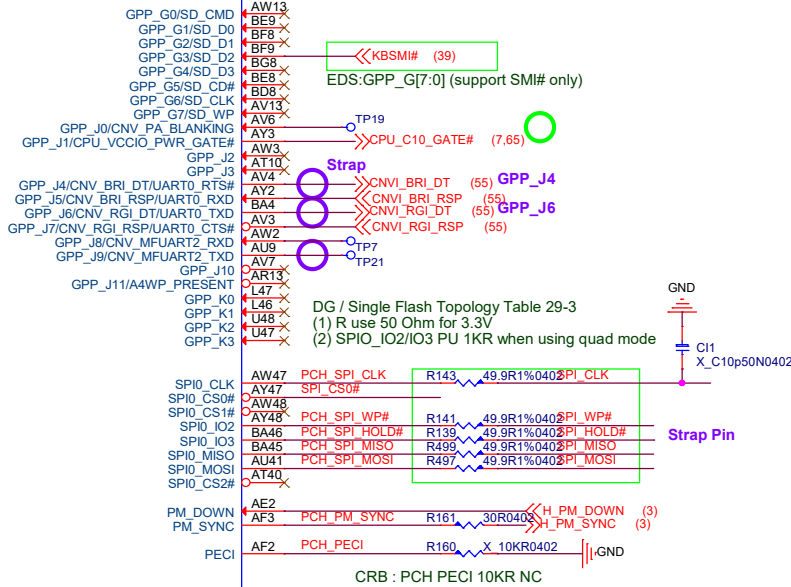
msi

MICRO-STAR INT'L CO.,LTD.

Title				
PCH-4(HDA/GPIO/TJAG)				
Size	Document Number			Rev
Customer	MS-16Q2			10
Date:	Thursday, January 25, 2018	Sheet	35 of 73	



U13E



CRB : PCH PEGI 10KR NC

GPP\_J4

GPP\_J6

GPP\_J9

SPI0\_IO2

SPI0\_IO3

SPI0\_MOSI

## MISO isn't Strap

[illegible]

M31-2512893-W03  
M-IC FLASH, 128M(16Mx8bit), 10ms, SOIC-8pin(208mil), WINBOND/W25Q128JVSQI, 2.7V, 3.6V, SPI,, HALOGEN FREE

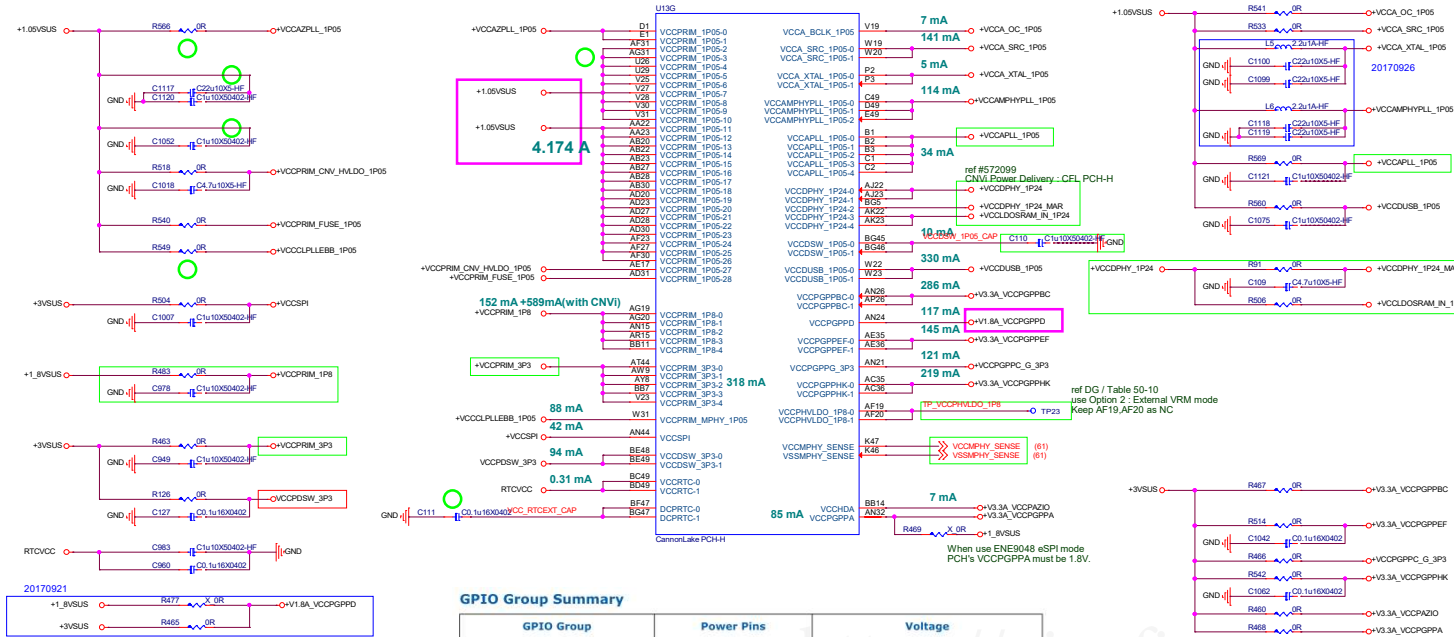
M31-2512832-M24  
M-IC FLASH, 128M(16Mx8bit), 40ms, SOP-8pin, MXICMX25L12873FM2I-10G(T), 2.7V, 3.6V, SPI,, HALOGEN FREE

Title			
<b>PCH-5(UART/I2C/SPI)</b>			
Size	Document Number	Rev	
	<b>MS-16Q2</b>	<b>10</b>	
Date:	Thursday, January 25, 2018	Sheet	36 of 73



# HM370 (Power)

ref DG / Table 50-6 Decoupling Requirements



## GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPBC	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPD	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPEF	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPG_3P3	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPHK	1.8V or 3.3V
Primary Well Group G (GPP_G)	VCCPRIM_3P3 or VCCPRIM_1P8	1.8V or 3.3V
Primary Well Group H (GPP_H)	VCCDSW_3P3	1.8V or 3.3V
Primary Well Group I (GPP_I)	VCCPRIM_3P3	3.3V Only
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only

**Note:** Except for GPP\_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP\_G group voltage is selected by setting the corresponding soft strap only.

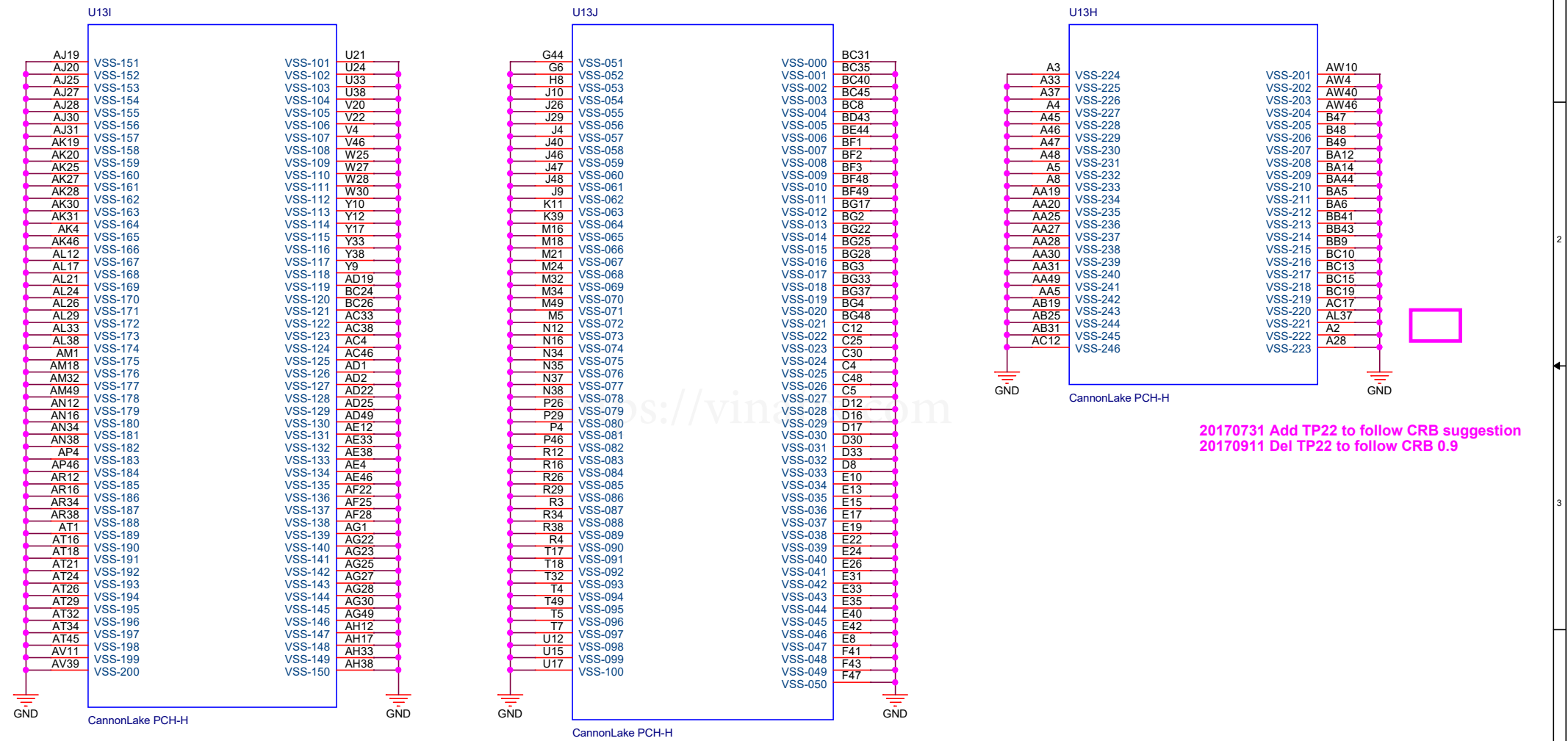
Vinafix.com

## Power Descriptions for PCH in CNL-H

Name	Description
VCCA_BCLK_1P05	Analog supply for BCLK circuitries: 1.05V
VCCA_SRC_1P05	Analog supply for PCIe clock circuitries: 1.05V
VCCA_XTAL_1P05	Analog supply for XTAL circuitries: 1.05V
VCCDUSB_1P05	Supply for USB digital logic: 1.05V
VCCAPLL_1P05	Analog supply for BCLK/DMT/Audio PLLs: 1.05V. This rail can be derived from the VCCPRIM_1P05 rail with the proper isolation. Refer to the Platform Design Guide for implementation detail.
VCCPRIM_1P05	Primary Well: 1.05V. For PCIe/USB3/SATA MPHY logic, I/O blocks, SRAM, JTAG, CNVI.
VCCDSW_1P05	Deep Sx Well: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect a 1uF capacitor to this rail and power should NOT be driven from the board.
VCCPRIM_MPHY_1P05	Mod PHY Primary: 1.05V. Primary supply for PCIe/USB3/SATA MPHY logic and PCIe/USB PLL dividers.
VCCMPHYPLL_1P05	Analog supply for USB3, PCIe Gen 2/Gen 3, and SATA3 PLLs: 1.05V. Refer to the Platform Design Guide for filtering and decoupling recommendations.
VCCPRIM_1P8	1.8V Primary Well.
VCCPRIM_3P3	3.3V Primary Well.
VCCSPI	SPI Primary Well 3.3V or 1.8V. for SPI interface.
VCCCHA	HDA Audio Power 3.3V, 1.8V, or 1.5V. for Intel's High Definition Audio.
VCCDSW_3P3	3.3V Deep Sx Well.
VCCRTC	RTC Well Supply. This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained. <b>Note:</b> VCCRTC nominal voltage is 3.0V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. Refer to the Platform Design Guide, RTC Design Guidelines chapter for latest design recommendations. <b>Note:</b> Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
DCPRTC	RTC decoupling capacitor only. This rail should NOT be driven.
VCCDPHY_1P24	1.24V for CNVI logic. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide for implementation details.
VCCDPHY_EC_1P24	For decoupling capacitor only. This rail should NOT be driven from the motherboard. This rail can optionally be connected to VCCDPHY_1P24 on the motherboard.
VCCPHVDDO_1P8	1.8V Primary Well. On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCPGPPA	1.8V or 3.3V for GPP_A group.
VCCPGPPBC	1.8V or 3.3V for GPP_B and GPP_C groups.
VCCPGPPD	1.8V or 3.3V for GPP_D group.
VCCPGPPEF	1.8V or 3.3V for GPP_E and GPP_F groups.
VCCPGPPG_3P3	3.3V for GPP_G group.
VCCPGPPHK	1.8V or 3.3V for GPP_H and GPP_K groups.
VCCMPHY_SENSE	1.05V Sense Line.
VSSMPHY_SENSE	0V (Ground) Sense Line.
VSS	Ground.



# PCH-H(GND)





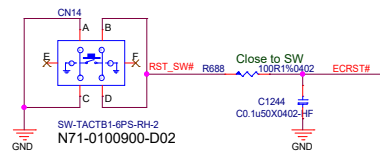
## KBC/EC/uP (ENE9028)

### ENE9028 & 9048 Power Notes :

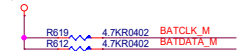
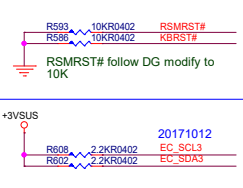
pin9 VCCLPC :  
3.3V for ENE9028's LPC mode.  
1.8V for ENE9048's eSPI mode.

pin111 VCC0 :  
3.3V for ENE9028's PLC function  
3.3V for ENE9048's eSPI operation with Pre-Driver.

## Hardware Reset

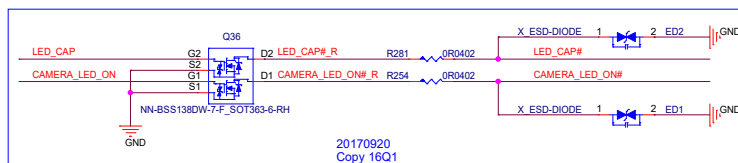
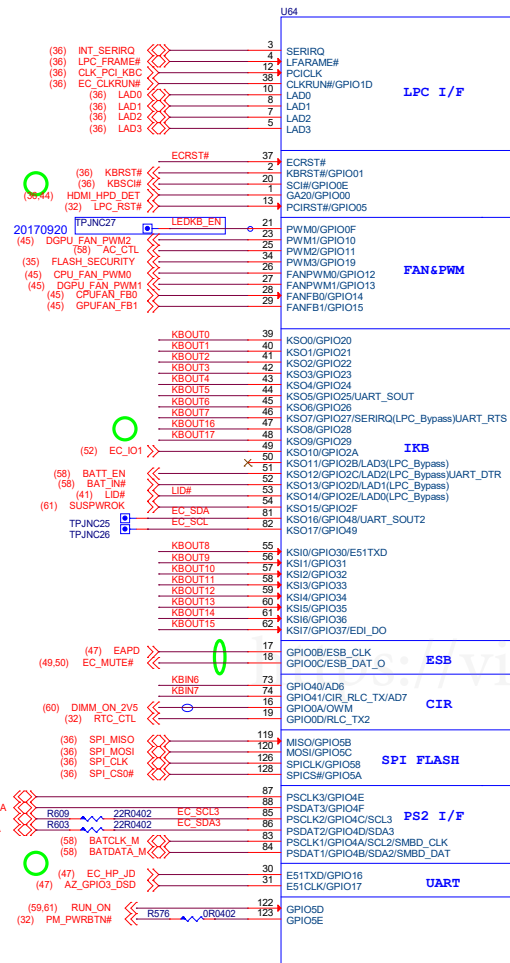
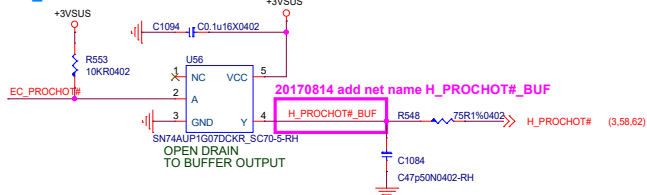


**PU/PD**

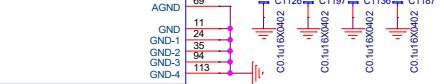


20170829 add R3528

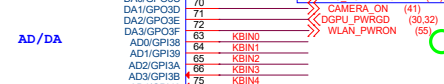
## EC\_PROCHOT#



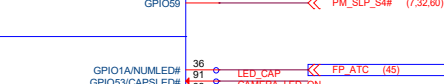
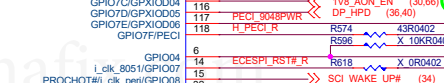
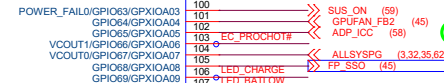
## POWER/GROUND



---

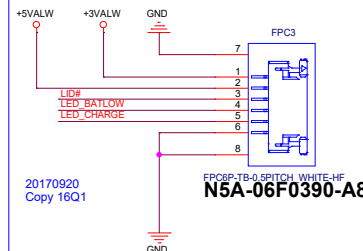


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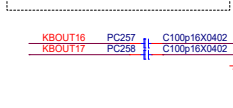
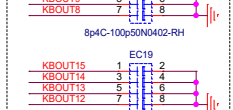
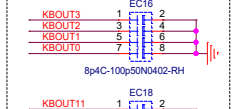
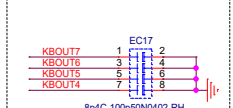



LED

## LED Board



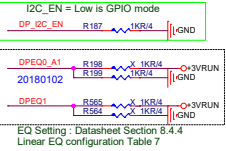
**For EMI**



 <b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b> <b>KBC/EC/uP (ENE9028)</b>	
<b>Size</b> <b>Custom</b>	<b>Document Number</b> <b>MS-16Q2</b>
<b>Rev</b> <b>10</b>	

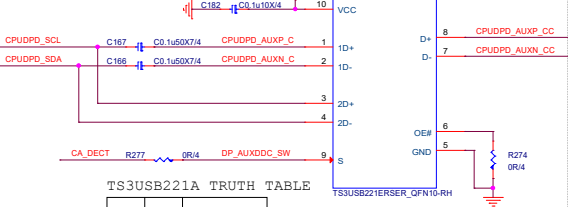


DP 1.4 Redriver (TUSB546-DCI)

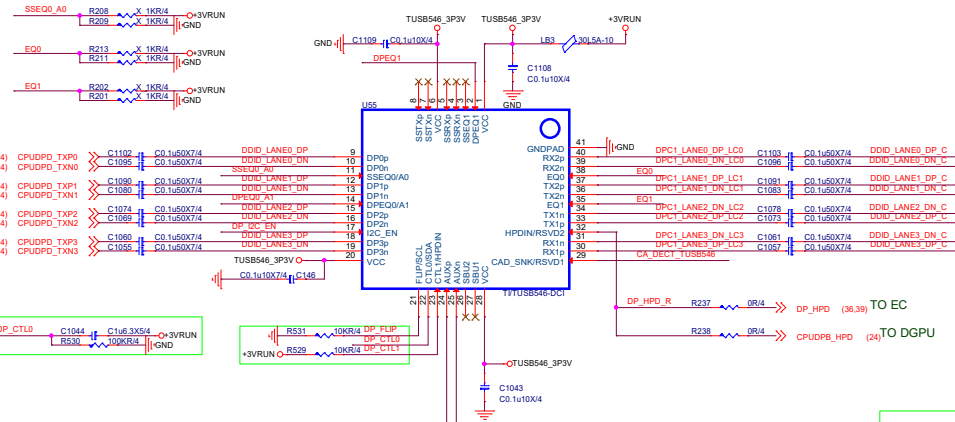
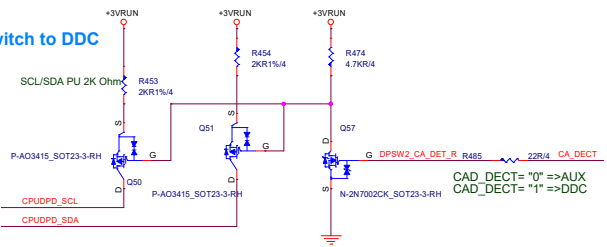


REF	CPUG	CPUL	Mux Operation
1	LOW	LOW	POWER DOWN
2	LOW	HIGH	4-lane Orientation 1
3	HIGH	LOW	4-lane Orientation 2
4	LOW	HIGH	2-lane Orientation 1
5	HIGH	HIGH	2-lane Orientation 2
6	LOW	LOW	USB3.1 only Orientation 1
7	HIGH	HIGH	USB3.1 only Orientation 2

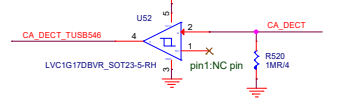
AUX/DDC Switch



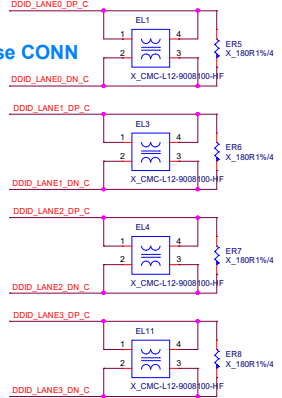
For Dual Mode Switch to DDC



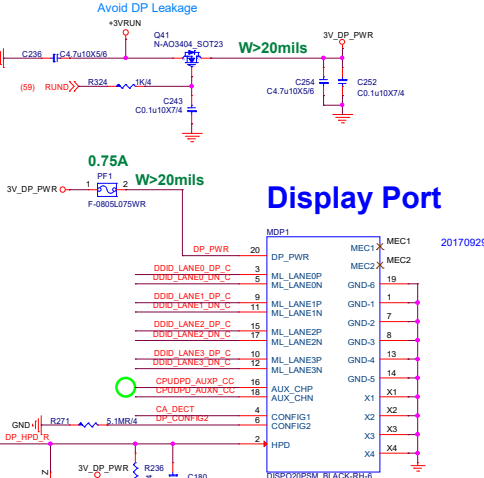
Buffer for CAD SNK



EMI Close CONN

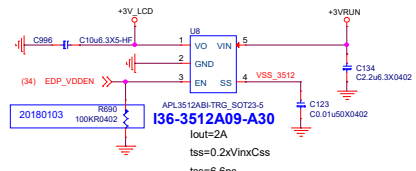


Display Port

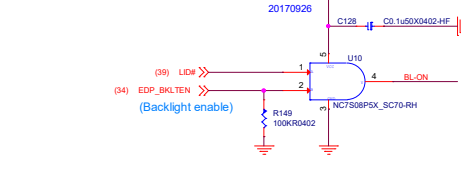




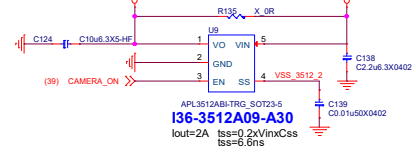
## Pannel Device Logic Power



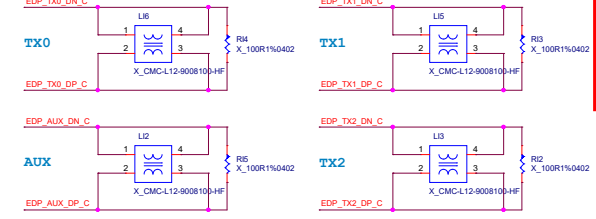
## Backlight



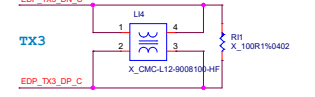
## CAMERA Power



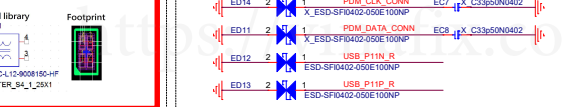
## EMI Close Connector



**Note:** CMC-L12-9008100-HF (P/N: L12-9008100-HF) is not match datasheet. Default ground library and footprint F11709\_04\_1\_23x1 are not match datasheet.



## ESD



## eDP Connector



## LCD Module Pin Define FOR FULL HD PANEL

Pin No	Symbol	Description
1	Vcom_SDA	Vcom IIC SDA
2	H_GND	High Speed Ground
3	LAN1_N	Complement Signal-Lane 1
4	LAN1_P	True Signal-Main Lane 1
5	H_GND	High Speed Ground
6	LAN0_N	Complement Signal-Lane 0
7	LAN0_P	True Signal-Main Lane 0
8	H_GND	High Speed Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	Power Supply +3.3 V (typical)
13	LCD_VCC	Power Supply +3.3 V (typical)
14	NC	No Connection (Reserved for CMI test)
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL_Enable Signal of LED Converter
23	BL_PWM	PWM Dimming Control Signal of LED Converter
24	Vcom_SCL	Vcom IIC SCL
25	NC	No Connection (Reserved)
26	LED_VCCS	BL Power
27	LED_VCCS	BL Power
28	LED_VCCS	BL Power
29	LED_VCCS	BL Power
30	NC	No Connection (Reserved)

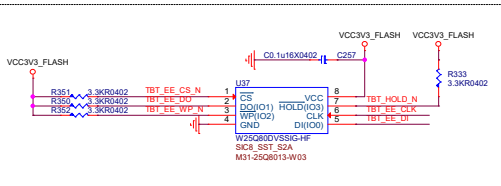
## LCD Module Pin Define FOR WQHD PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	VDD	
19	VDD	
20	VDD	
21	VDD	
22	BIST	BIST patterns selection L : Disable (default) , H : Enable
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE	Backlight On/Off
33	BL_PWM_DIM	System PWM
34	NC	Reserved for LCD manufacturer's use
35	NC	Reserved for LCD manufacturer's use
36	VBL	Backlight power
37	VBL	Backlight power
38	VBL	Backlight power
39	VBL	Backlight power
40	NC	No Connection (Reserved)



Vinafix.com

20170830  
R228 R232 change to 2.2K to follow CRE



20170830  
R228,R232 change to 2.2K to follow CRE

R289 2.2KR0402 TBT\_I2C\_SCL

R269 10KR0402 TBT\_CIO\_PLUG\_EV


R613	X	10KR0402	RTD3_USB_PWR_EN
R598	X	10KR0402	RTD3_CIO_PWR_EN

Pull-Hi HDMI

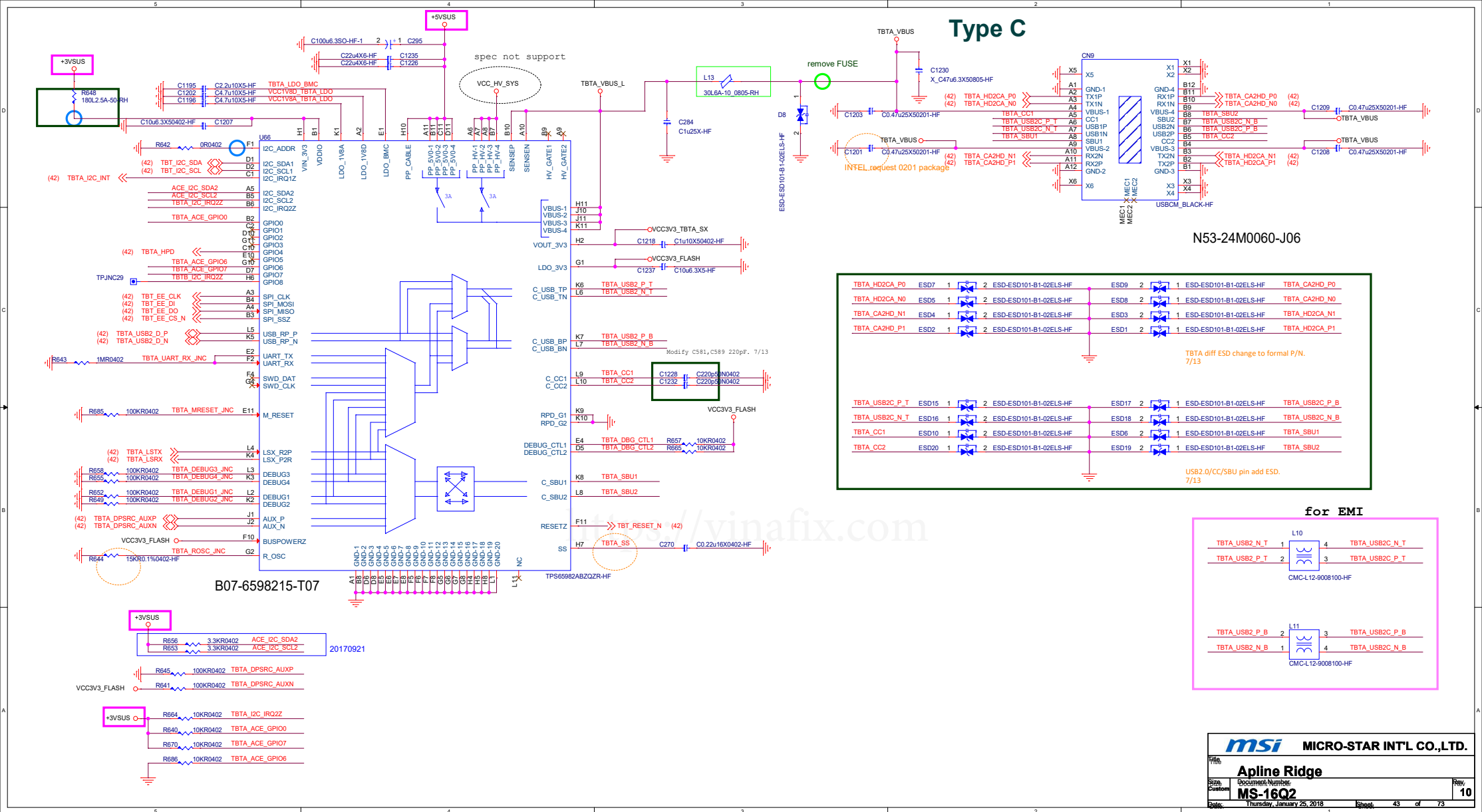
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20170919  
R461 change to connect with TBT\_CLKREQ#\_R

3

		MICRO-STAR INT'L CO.,LTD.	
Title <b>Alpine Ridge(TBT)</b>			
Size	Document Number <b>MS-16Q2</b>		Rev <b>10</b>
Date:	Thursday, January 25, 2018	Sheet	42 of 73





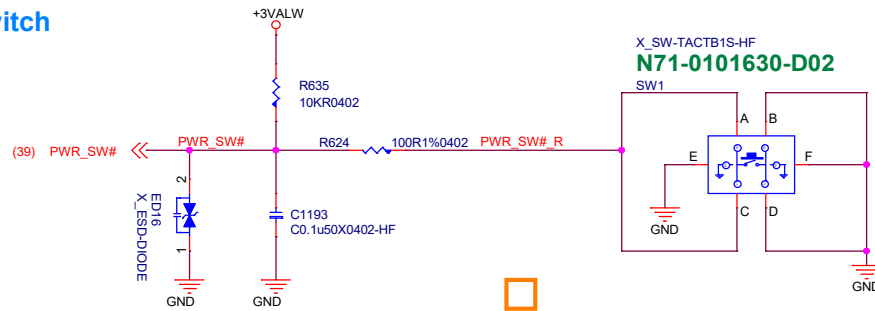




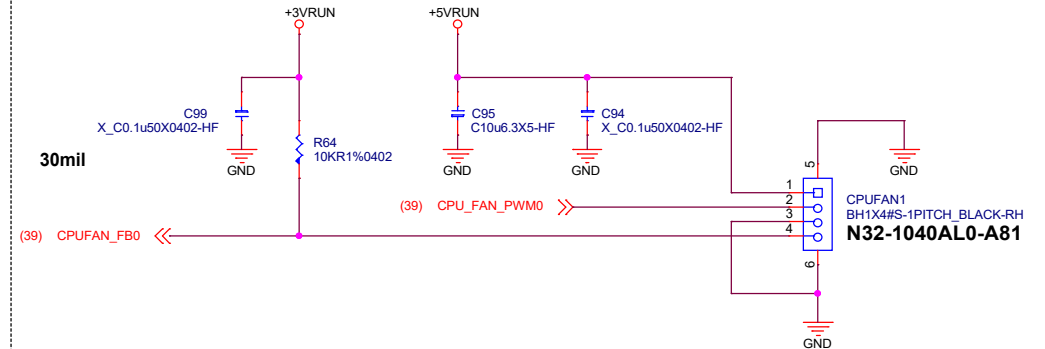


# PWR SW/CPU FAN/BTB CONN/ LED CONN

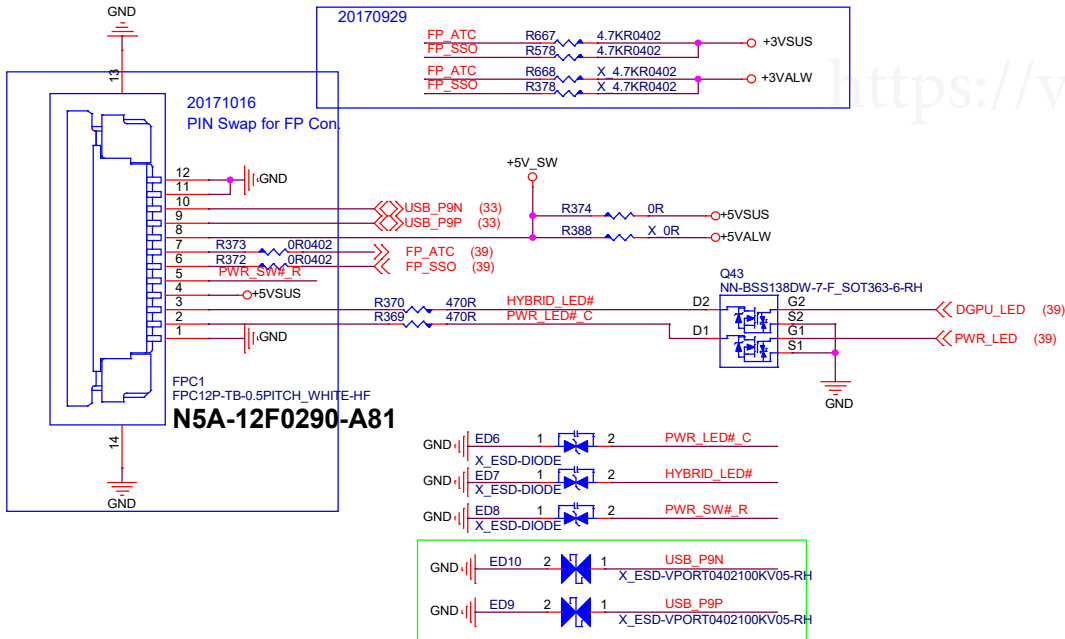
## Power Switch



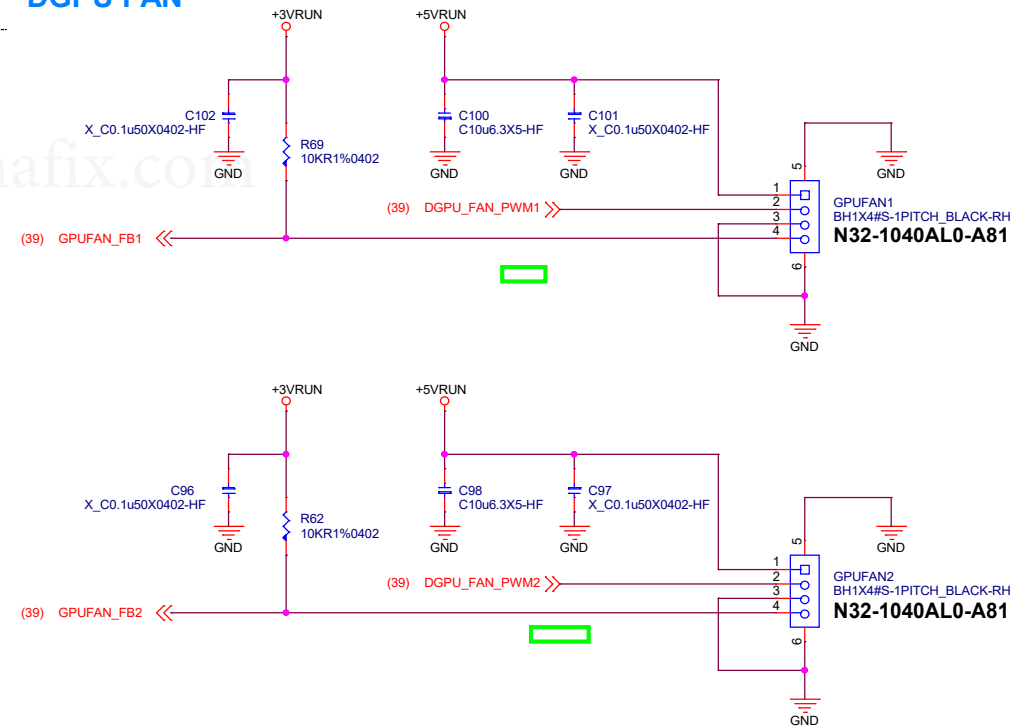
## CPU FAN



## Power LED+SW+FP

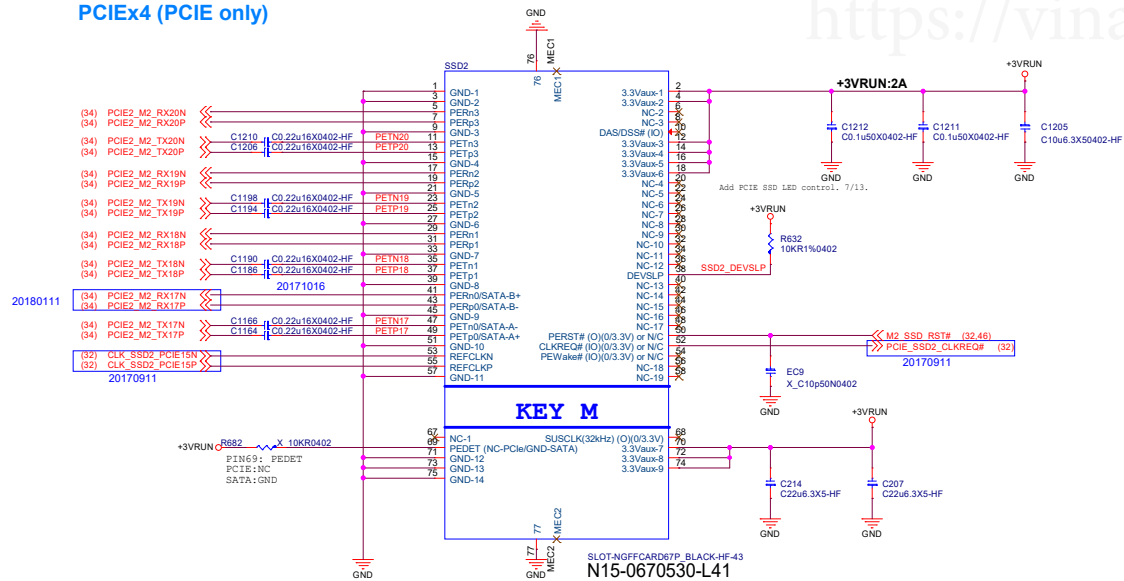


## DGPU FAN





M2 SSD -2  
PCIEx4 (PCIe only)





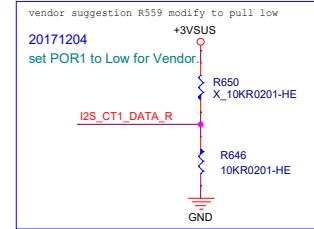
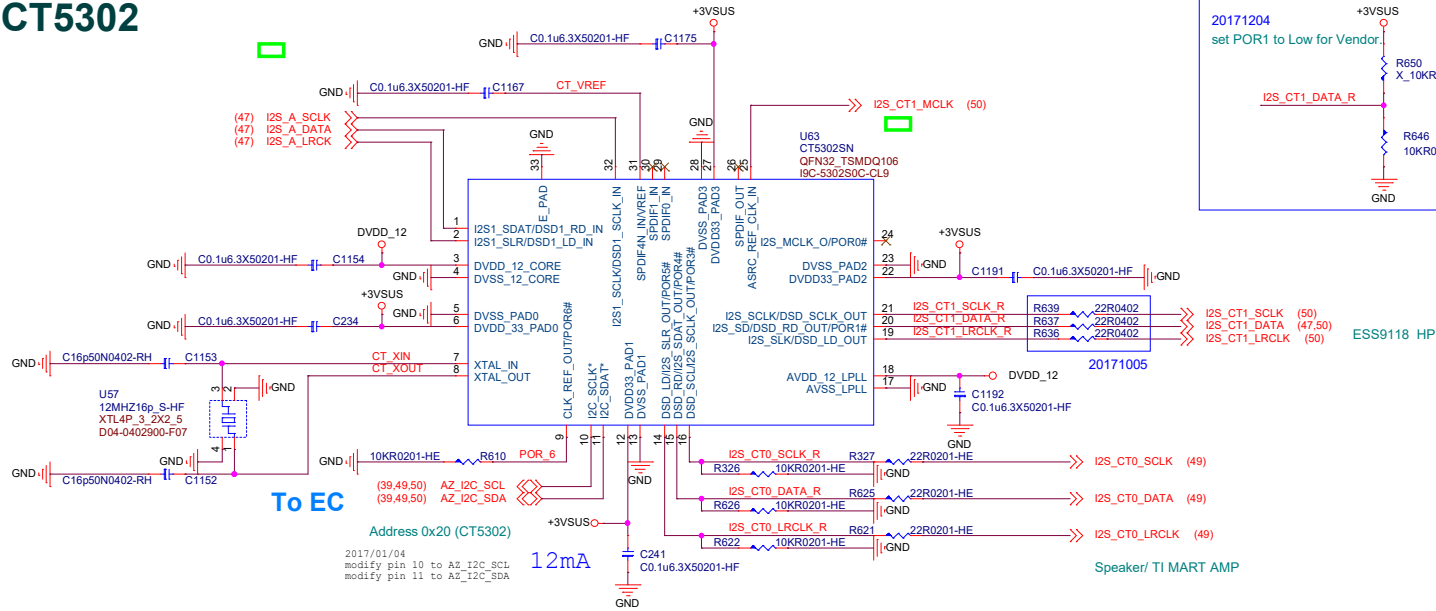
ALC1220	AZ_GPIO3_DSD
PCM DSD	H L



JACK	EARPHONE_JD
Insert	1
Pull Out	0



# CT5302



HW SETTING

HW SETTING

HW SETTING

**I2S output slave mode:**

Select I2S1 output port

No.	POR1	Definition
0	0	I2S output master mode
1	1	I2S output slave mode

**Hardware Crystal:**

Select current external crystal frequency

No	POR4	POR3	Definition
0	0	0	12.0000MHz
1	0	1	11.2896MHz
2	1	0	12.2880MHz
3	1	1	14.3180MHz

**I2C Slave ID**

Define chip I2C slave address

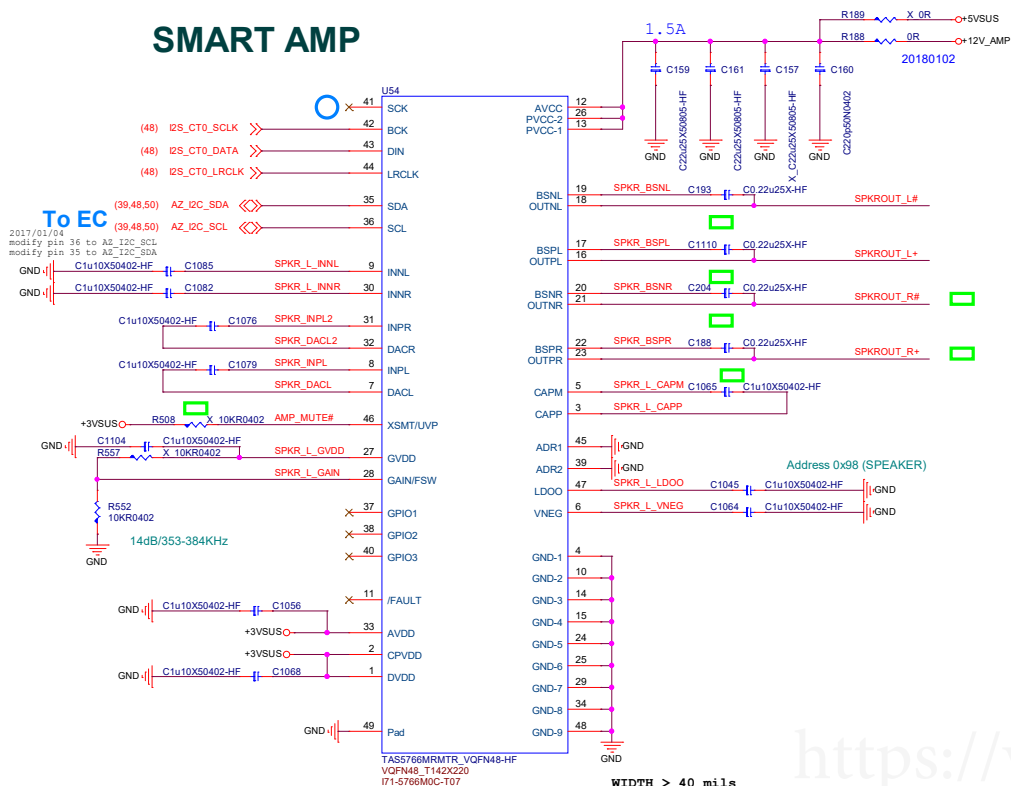
No	POR6	POR5	Definition
0	0	0	0x20
1	0	1	0x22
2	1	0	0x24
3	1	1	0x26

Pin Name	Description	Function Table
POR_IN_1	POWER_ON_LATCH_DC[1] = SEL_I2S_TX_SLAVE_MODE	Select I2S1 output port is master or slave mode
POR_IN_3	POWER_ON_LATCH_DC[4:3] = SEL_XTAL[1:0]	Select Crystal frequency
POR_IN_4		
POR_IN_5	POWER_ON_LATCH_DC[6:5] = I2C_ID[1:0]	I2C serial interface device ID selection
POR_IN_6		

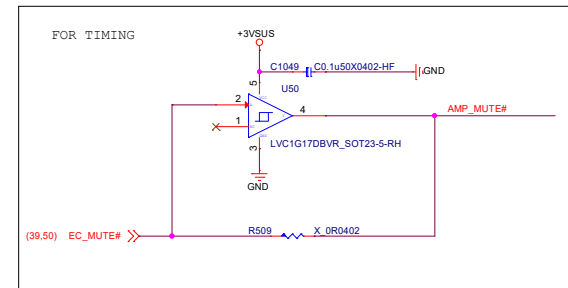


# SMART AMP

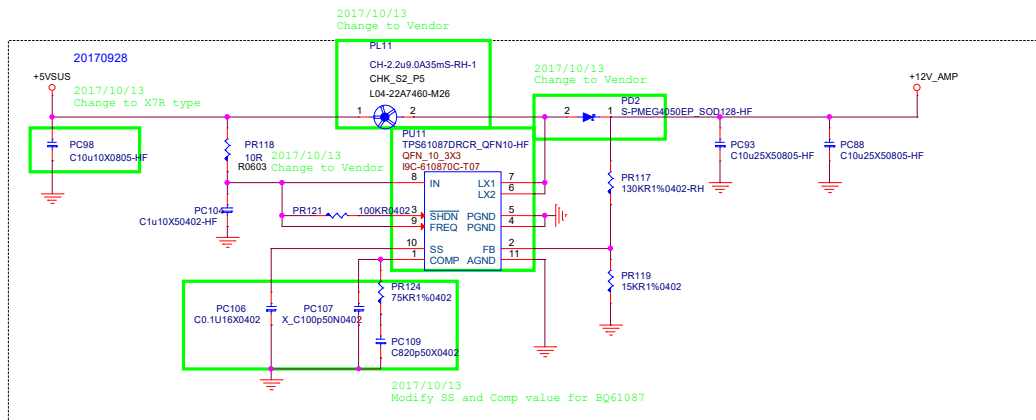
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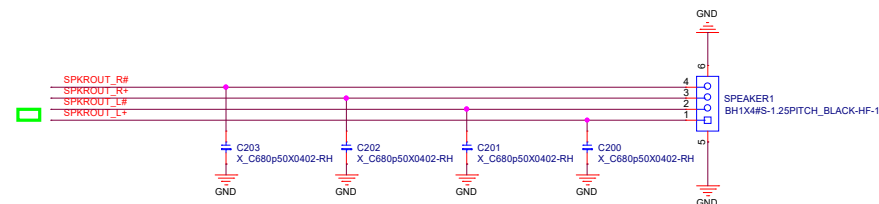
WIDTH > 40 mils



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CON TO BE CONFIRM  
SPK Conn





The image contains three circuit diagrams, each showing a different method to implement a voltage divider for a 5V regulator. Each diagram includes a 5V regulator (U65, U35, U27) and a 5V output (VOUT).

**Diagram 1 (Top):** A 5V regulator (U65) is shown with its input (VIN) connected to a 5V source (+5VSUS) through a 10k resistor (R244). The output (VOUT) is connected to a 5V output (+5VOUT) through a 10k resistor (R672). The output is also connected to a 5V output (+5VOUT) through a 10k resistor (R672). The output is also connected to a 5V output (+5VOUT) through a 10k resistor (R672).

**Diagram 2 (Middle):** A 5V regulator (U35) is shown with its input (VIN) connected to a 5V source (+5VSUS) through a 10k resistor (R255). The output (VOUT) is connected to a 5V output (+5VOUT) through a 10k resistor (R337). The output is also connected to a 5V output (+5VOUT) through a 10k resistor (R337). The output is also connected to a 5V output (+5VOUT) through a 10k resistor (R337).

**Diagram 3 (Bottom):** A 5V regulator (U27) is shown with its input (VIN) connected to a 5V source (+5VSUS) through a 10k resistor (R285). The output (VOUT) is connected to a 5V output (+5VOUT) through a 10k resistor (R307). The output is also connected to a 5V output (+5VOUT) through a 10k resistor (R307). The output is also connected to a 5V output (+5VOUT) through a 10k resistor (R307).

The output voltage is calculated as:

$$V_{out} = (1 + (12.7k / 10.2k)) \cdot 0.8 = 1.796V$$

**From EC**

(39,49) EC\_MUTE#

**To HP SW**

HP\_MUTE

**HP JACK**

(47) HP\_SEL

**FROM REALTEK**

HP\_SEL\_R

HP\_SEL\_E

HP\_DIR\_SEL

**ESS OUT**

**ALC1220 IN**

**U39**

ISL54405IRUZ-T\_UTOFN16-RH

TOFN16

I94-544050C-111

**Q67**

N-2N7002CK\_SOT23-3-RH

SOT23SGD\_T

D03-07002F9-N47

**R681**

100KR0402

**R687**

X\_10KR1%0402

**R343**

0R

**R349**

10KR0201-HE

**R362**

0R0402

**R355**

10KR0201-HE

**R348**

10KR0201-HE

**C282**

C0.1u10X0402

**C279**

C0.1u10X0402

**U39**

ISL54405IRUZ-T\_UTOFN16-RH

TOFN16

I94-544050C-111

**Q67**

N-2N7002CK\_SOT23-3-RH

SOT23SGD\_T

D03-07002F9-N47

**U39**

ISL54405IRUZ-T\_UTOFN16-RH

TOFN16

I94-544050C-111

**SEL**

0

1

**L1 / R1**

L2 / R2

**Earphone Impedance**

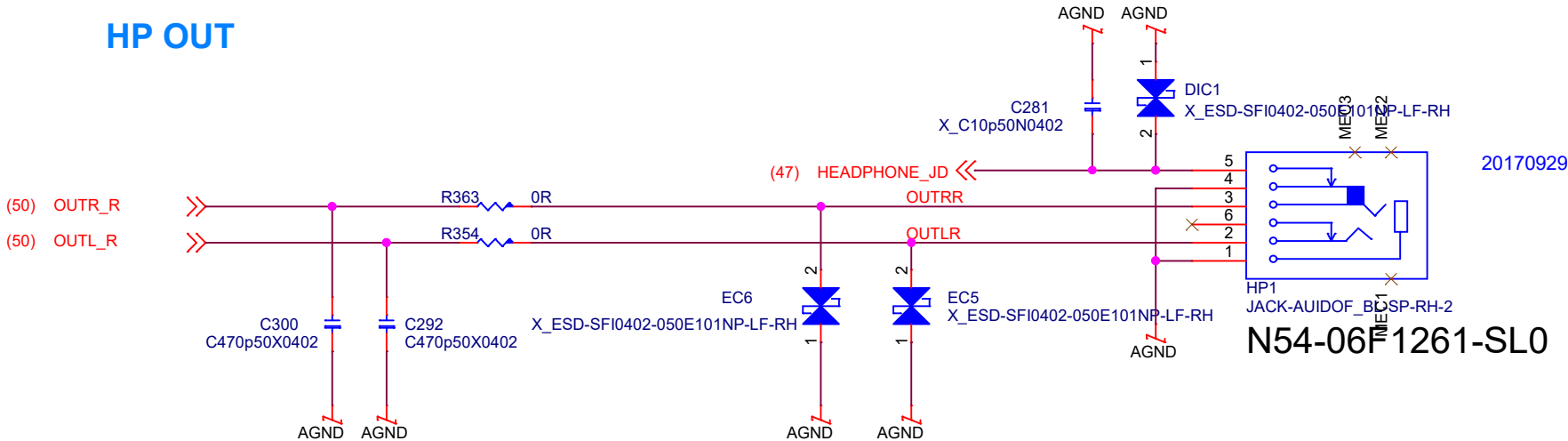
INPUTS				OUTPUTS				
AC/DC	DIR	MUTE	SEL	L1, R1	L2, R2	COM (L/R) C/P Shunts	L1, R1 C/P Shunts	L2, R2 C/P Shunts
0	X	0	0	ON	OFF	OFF	OFF	OFF
0	X	0	1	OFF	ON	OFF	OFF	OFF
0	X	1	X	OFF	OFF	OFF	OFF	OFF
1	0	0	0	ON	OFF	OFF	OFF	ON
1	0	0	1	OFF	ON	OFF	ON	OFF
1	0	1	X	OFF	OFF	OFF	ON	ON
1	1	0	0	ON	OFF	OFF	OFF	ON
1	1	0	1	OFF	ON	OFF	OFF	ON
1	1	1	X	OFF	OFF	ON	OFF	OFF

NOTE: MUTE, AC/DC, DIR: Logic "0"  $\leq 0.5V$ , Logic "1"  $\geq 1.4V$  or Float with a 3.3V Supply or 5V supply.  
SEL: Logic "0"  $\leq 0.5V$ , Logic "1"  $\geq 1.4V$  with a 3.3V Supply or 5V supply.  
X = Don't Care

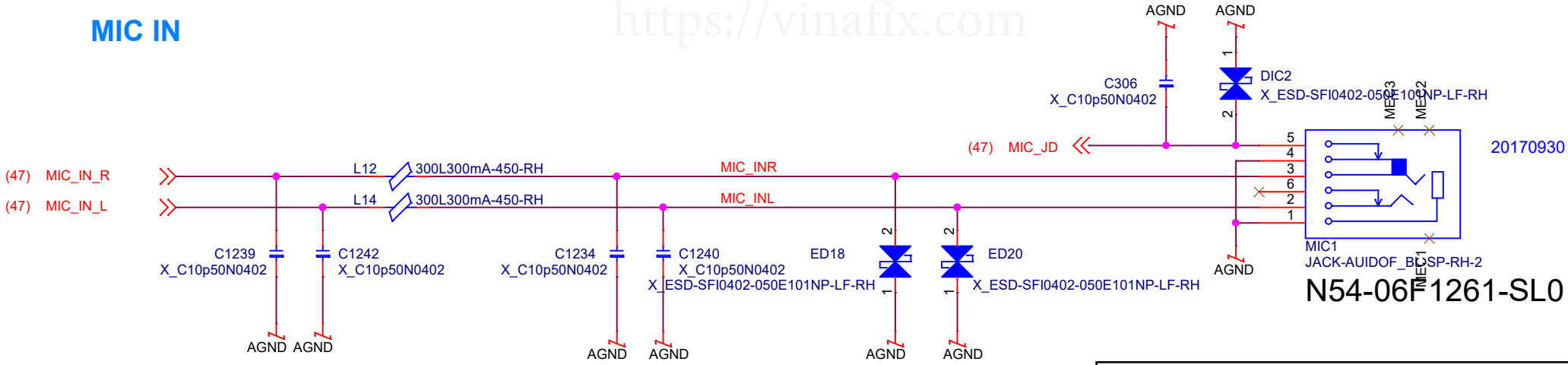


# Audio CONN

## HP OUT



## MIC IN



<b>msi</b> MICRO-STAR INT'L CO.,LTD.	
Title	
Audio Jack	
Size	Document Number
Custom	MS-16Q2
Date:	Thursday, January 25, 2018
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	PWM1	PWM2	PWM3	PWM4	PWM5
MCU_C1_EN					
MCU_C2_EN		P			F3
MCU_C3_EN			PgUp	F4	INS
MCU_C4_EN					
MCU_C5_EN		RIGHT	UP	DOWN	LEFT
MCU_C6_EN		F5	PgDn	F6	DEL
MCU_C7_EN	F8	CAP	A	S	D
MCU_C8_EN	F9	TAB	Q	W	E
MCU_C9_EN	F10	CTRL_L	WIN_L	ALT_L	K131
MCU_C10_EN	F11	SHI_L	\\(K45)	Z	X
MCU_C11_EN	V	B	N	M	< ,
MCU_C12_EN	F12	SPACE	3#	K132	C
MCU_C13_EN	> .	/ ?	K56	SHI_R	ENT
MCU_C14_EN	K133	ALTR	SS (Fn)	2@	CTR_R
MCU_C15_EN	F	G	H	J	K
MCU_C16_EN	L	::	""	K42	\\(K29)
MCU_C17_EN	O	F7	{ [	} ]	BACK
MCU_C18_EN	R	T	Y	U	I
MCU_C19_EN	9 (	0)	_ -	+ =	k14
MCU_C20_EN	4\$	5%	6^	7&	8*
MCU_C21_EN	` ~	1!	ESC	F1	F2
MCU_C22_EN	PAUSE	SCR	PRT		
MCU_C23_EN					
MCU_C24_EN					
MCU_C25_EN					

Mapping to  
KBC's KBIN & KBOUT



KBIN_3,KBOUT_9	KBIN_6,KBOUT_5	KBIN_7,KBOUT_5	KBIN_7,KBOUT_4	KBIN_6,KBOUT_9
KBIN_3,KBOUT_5		KBIN_4,KBOUT_9	KBIN_5,KBOUT_9	
KBIN_1,KBOUT_12	KBIN_2,KBOUT_5	KBIN_6,KBOUT_12	KBIN_4,KBOUT_12	KBIN_2,KBOUT_12
KBIN_2,KBOUT_9	KBIN_4,KBOUT_5	KBIN_5,KBOUT_5	KBIN_5,KBOUT_4	KBIN_7,KBOUT_9
KBIN_6,KBOUT_4	KBIN_4,KBOUT_4	KBIN_1,KBOUT_4	KBIN_2,KBOUT_4	KBIN_0,KBOUT_4
KBIN_3,KBOUT_4		KBIN_7,KBOUT_12	KBIN_5,KBOUT_12	KBIN_3,KBOUT_12
	KBIN_0,KBOUT_13	KBIN_4,KBOUT_0	KBIN_5,KBOUT_0	KBIN_4,KBOUT_1
	KBIN_1,KBOUT_3	KBIN_2,KBOUT_0	KBIN_3,KBOUT_0	KBIN_2,KBOUT_1
	KBIN_3,KBOUT_3	KBIN_7,KBOUT_13	KBIN_4,KBOUT_3	KBIN_2,KBOUT_13
	KBIN_2,KBOUT_3	KBIN_0,KBOUT_9	KBIN_6,KBOUT_0	KBIN_7,KBOUT_0
KBIN_7,KBOUT_1	KBIN_6,KBOUT_2	KBIN_7,KBOUT_2	KBIN_6,KBOUT_6	KBIN_7,KBOUT_6
	KBIN_5,KBOUT_3		KBIN_5,KBOUT_13	KBIN_6,KBOUT_1
KBIN_6,KBOUT_7	KBIN_7,KBOUT_7	KBIN_6,KBOUT_8	KBIN_7,KBOUT_8	KBIN_1,KBOUT_5
KBIN_6,KBOUT_13	KBIN_6,KBOUT_3	KBIN_1,KBOUT_13	KBIN_3,KBOUT_13	KBIN_7,KBOUT_3
KBIN_5,KBOUT_1	KBIN_4,KBOUT_2	KBIN_5,KBOUT_2	KBIN_4,KBOUT_6	KBIN_5,KBOUT_6
KBIN_4,KBOUT_7	KBIN_5,KBOUT_7	KBIN_4,KBOUT_8	KBIN_5,KBOUT_8	KBIN_0,KBOUT_5
KBIN_2,KBOUT_7		KBIN_2,KBOUT_8	KBIN_3,KBOUT_8	KBIN_0,KBOUT_12
KBIN_3,KBOUT_1	KBIN_2,KBOUT_2	KBIN_3,KBOUT_2	KBIN_2,KBOUT_6	KBIN_3,KBOUT_6
KBIN_0,KBOUT_7	KBIN_1,KBOUT_7	KBIN_0,KBOUT_8	KBIN_1,KBOUT_8	KBIN_1,KBOUT_9
KBIN_1,KBOUT_1	KBIN_0,KBOUT_2	KBIN_1,KBOUT_2	KBIN_0,KBOUT_6	KBIN_1,KBOUT_6
		KBIN_0,KBOUT_10	KBIN_1,KBOUT_10	KBIN_2,KBOUT_10
	KBIN_0,KBOUT_3	KBIN_0,KBOUT_0	KBIN_1,KBOUT_0	KBIN_0,KBOUT_1
KBIN_0,KBOUT_11	KBIN_1,KBOUT_11	KBIN_2,KBOUT_11	KBIN_3,KBOUT_11	KBIN_4,KBOUT_11
KBIN_3,KBOUT_10	KBIN_4,KBOUT_10	KBIN_5,KBOUT_10	KBIN_6,KBOUT_10	KBIN_7,KBOUT_10
KBIN_3,KBOUT_7		KBIN_7,KBOUT_11	KBIN_6,KBOUT_11	KBIN_5,KBOUT_11



**msi**

**MICRO-STAR INT'L CO.,LTD.**

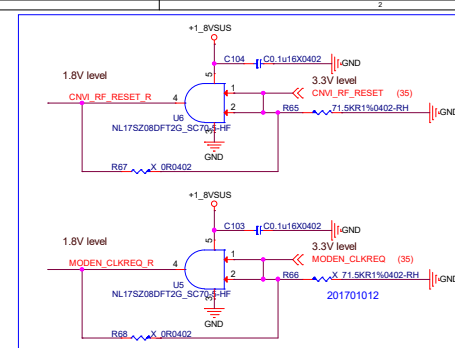
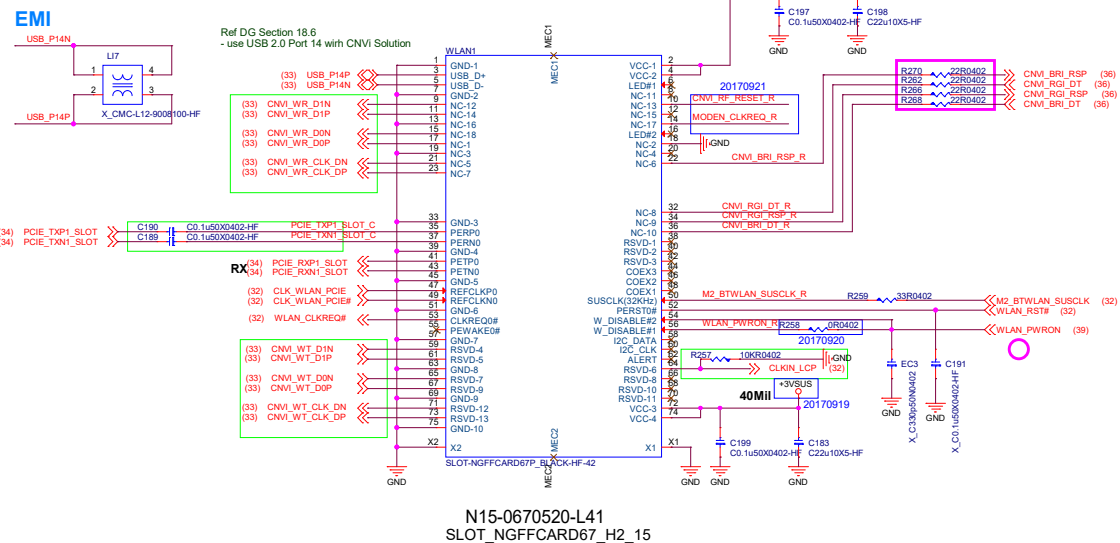
**Title**  
**Keyboard Matrix**

**Size**  
**Document Number**  
**MS-16Q2**

**Rev**  
**10**

**Date:** \_\_\_\_\_ **Sheet** 54 **of** 73





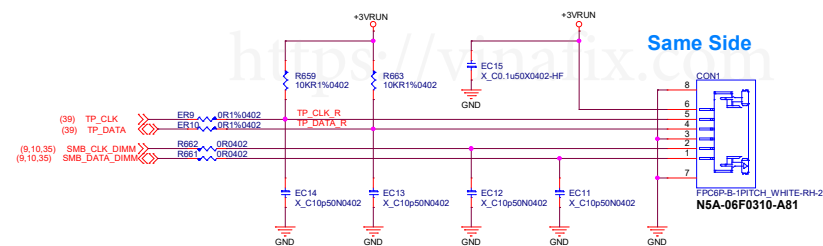
20170817 change R2394 stuff and  
R2397 unstuff for strap pin setting

GPP J4

This signal has a weak internal pull-down.  
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.  
0 = 38.4 XTAL frequency selected. (Default)  
1 = 24MHz XTAL frequency selected.

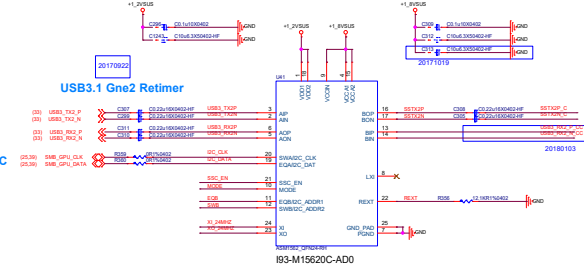
## GPP J6

An external pull-up or pull-down is required.  
0 = Integrated CNVi enable.  
1 = Integrated CNVi disable.

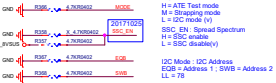




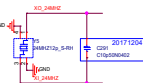
### USB3.1 Gne2 Retimer



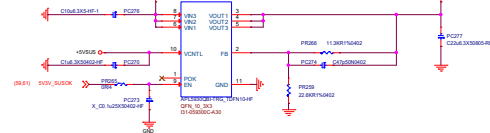
### Strap



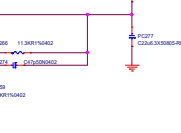
### 24MHz Clock



### +1\_2VSUS



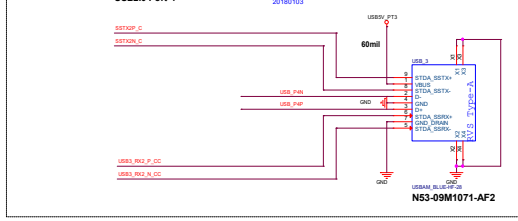
### MAX 1A



### USB3.0 CNT-3

### USB3.0 Port-2

### USB2.0 Port-4

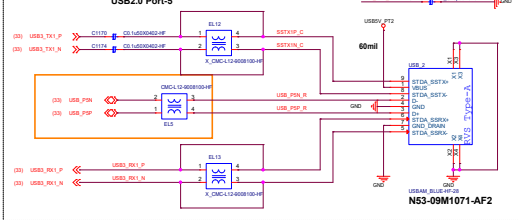


**Note:** CMC-L12-9008100-HF (P/N : L12-9008100-105) \*s  
Default Orcad library and footprint FILTER\_S4\_1\_25X1  
are not match datasheet.

### USB3.0 CNT-2

### USB3.0 Port-1

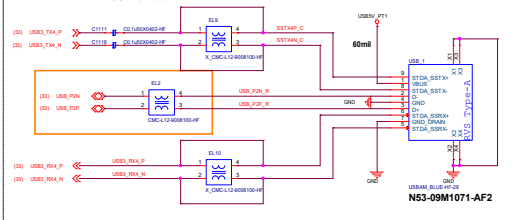
### USB2.0 Port-5



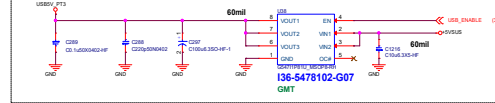
### USB3.0 CNT-1

### USB3.0 Port-4

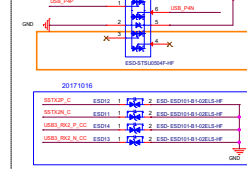
### USB2.0 Port-2



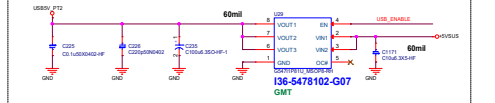
### USB Power Switch



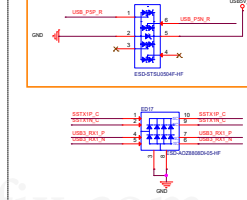
### ESD



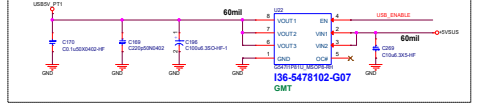
### USB Power Switch



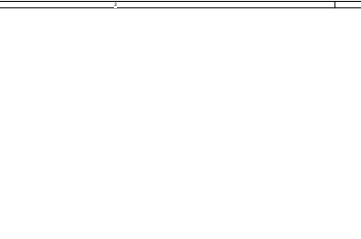
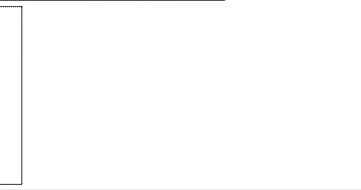
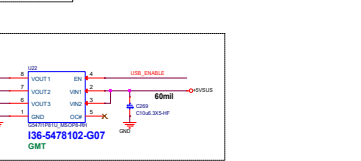
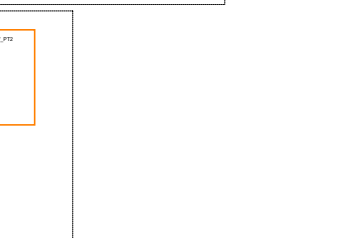
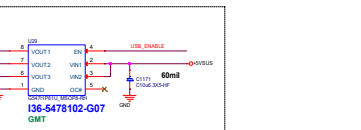
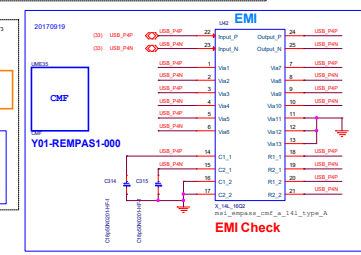
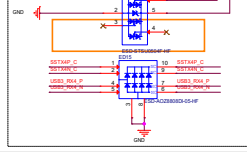
### ESD



### USB Power Switch

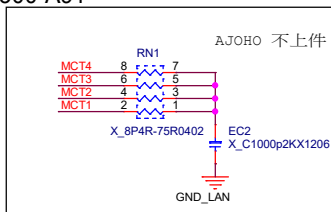
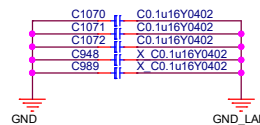
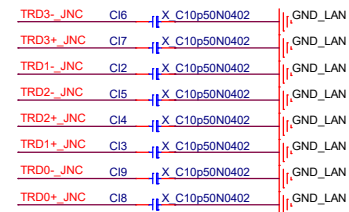
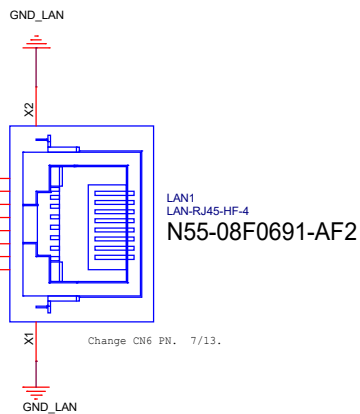
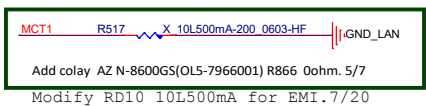
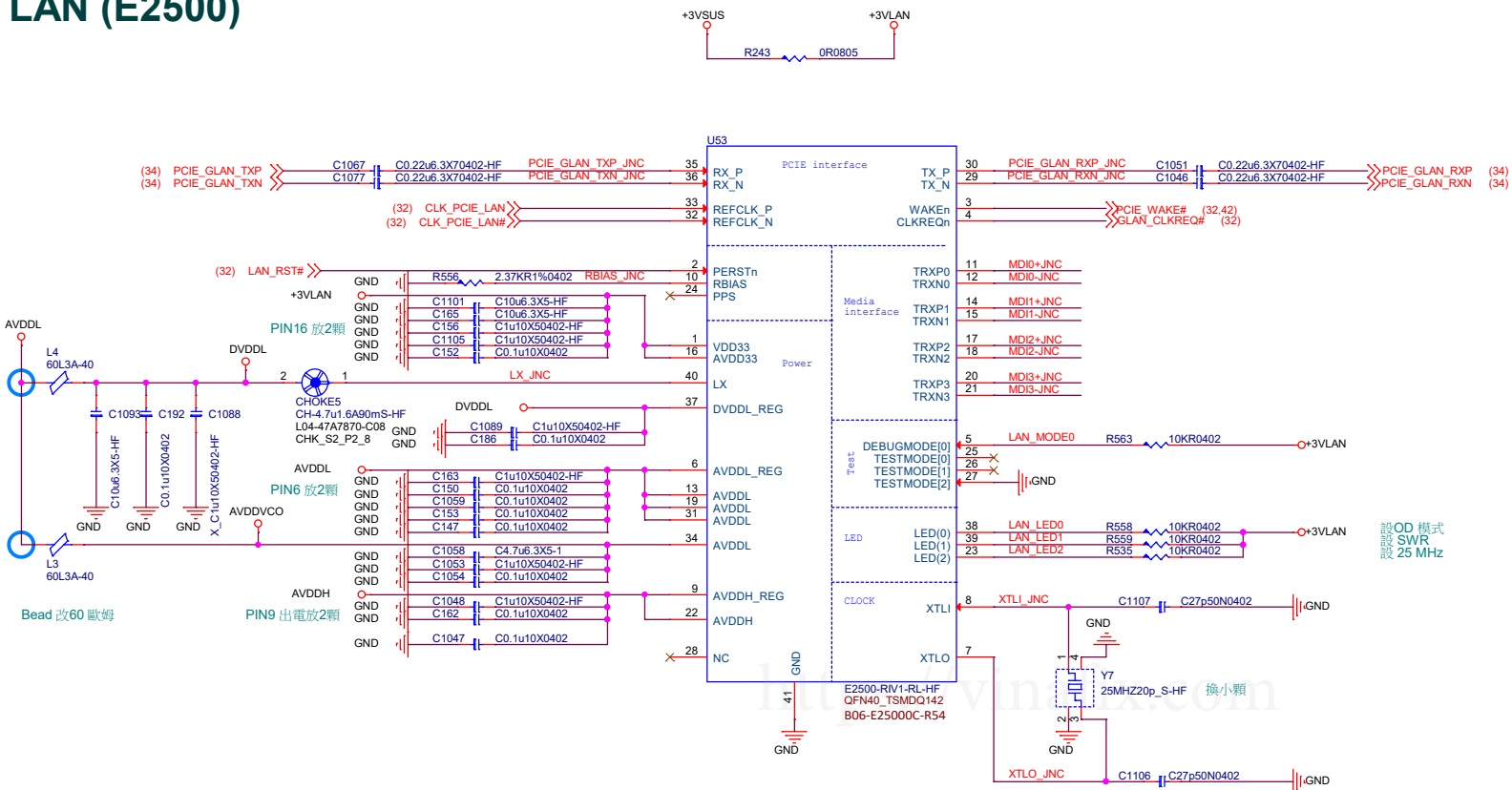


### ESD



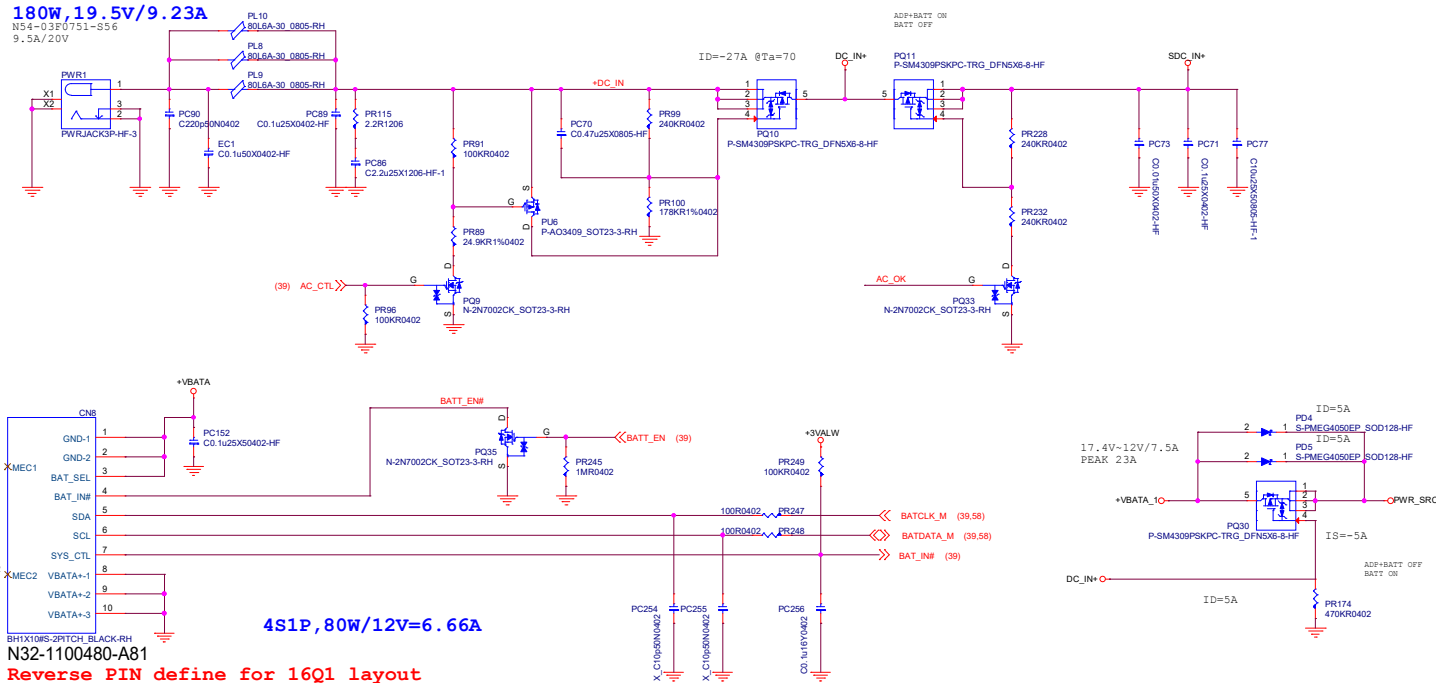


## LAN (E2500)

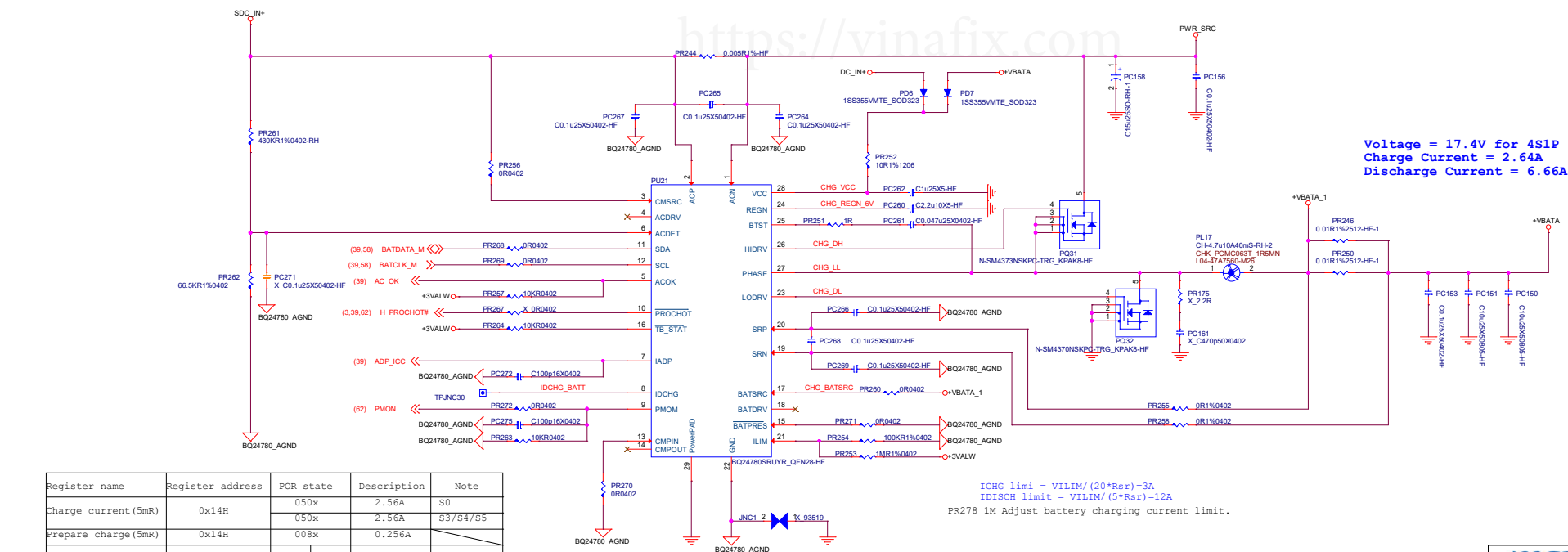
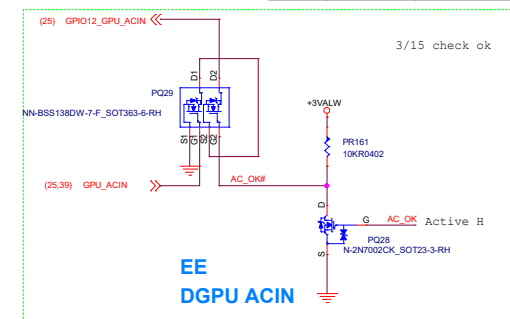




N92-03M0941-SLO  
180W, 19.5V/9.23A  
N54-03F0751-S56  
9.5A/20V



AC_OK#	GPU_ACIN (EC control)	GPIO12_GPU_ACIN
0	0	AC
0	1	AC
1	0	AC
1	1	DC



Register name	Register address	POR state	Description	Note
Charge current (5mR)	0x14H	050x	2.56A	S0
		050x	2.56A	S3/S4/S5
Prepare charge (5mR)	0x14H	008x	0.256A	
Input current (5mR)	0x3FH	19.5V 110x	8.704A	180W
Charge voltage	0x15H	43Fx	17.392V	4S1P
Discharge current (5mR)	0x39H	080x	4.096A	BOOST current

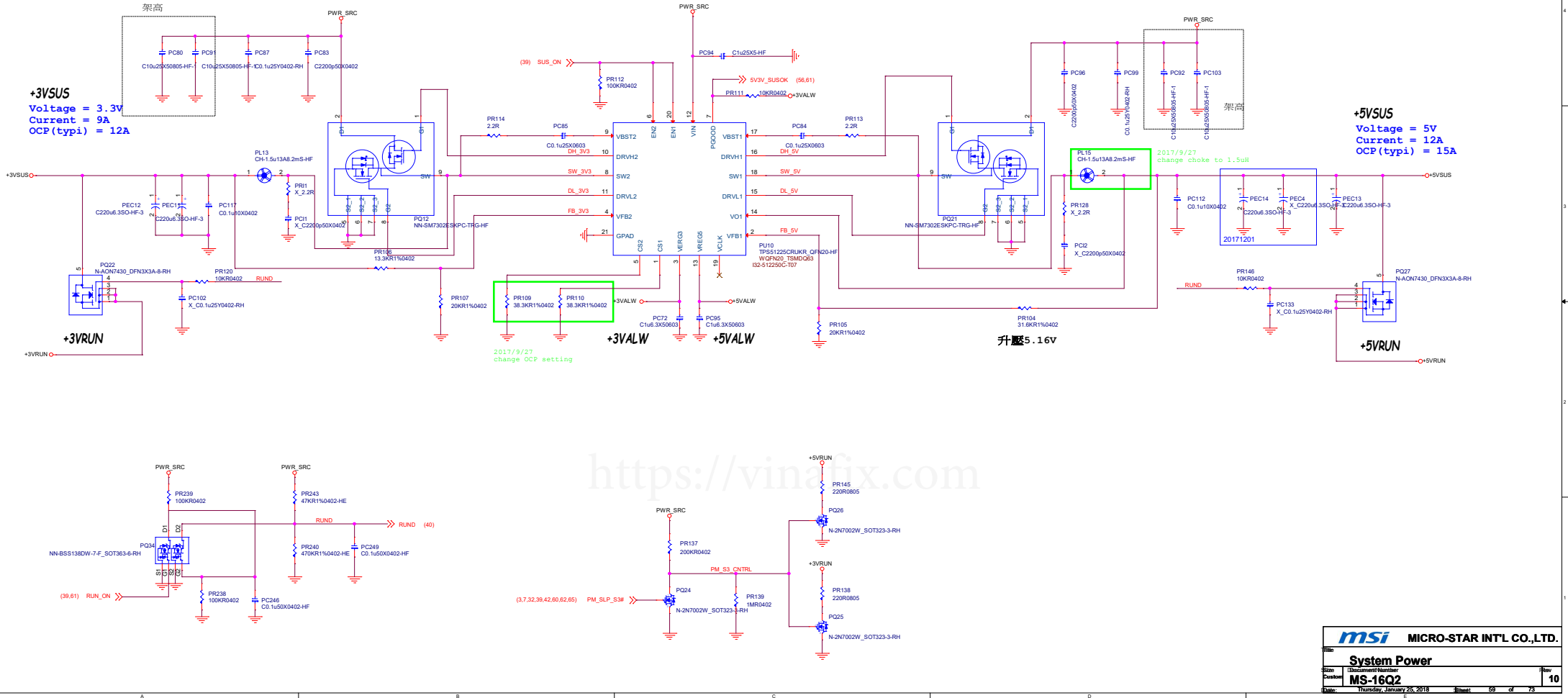
```

    ICHG limi = VILIM/(20*Rsr)=3A
    IDISCH limit = VILIM/(5*Rsr)=12A
PR278 1M Adjust battery charging current limit

```

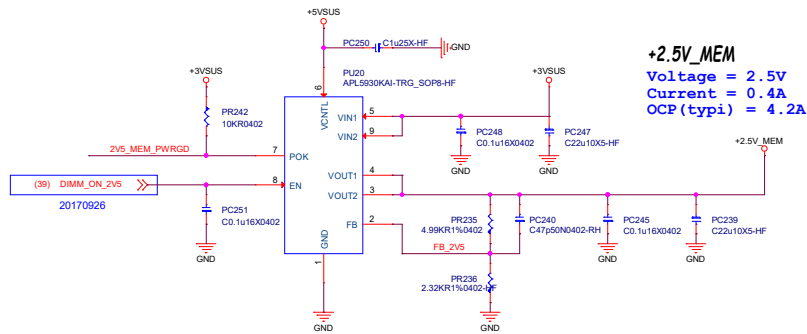


System Power

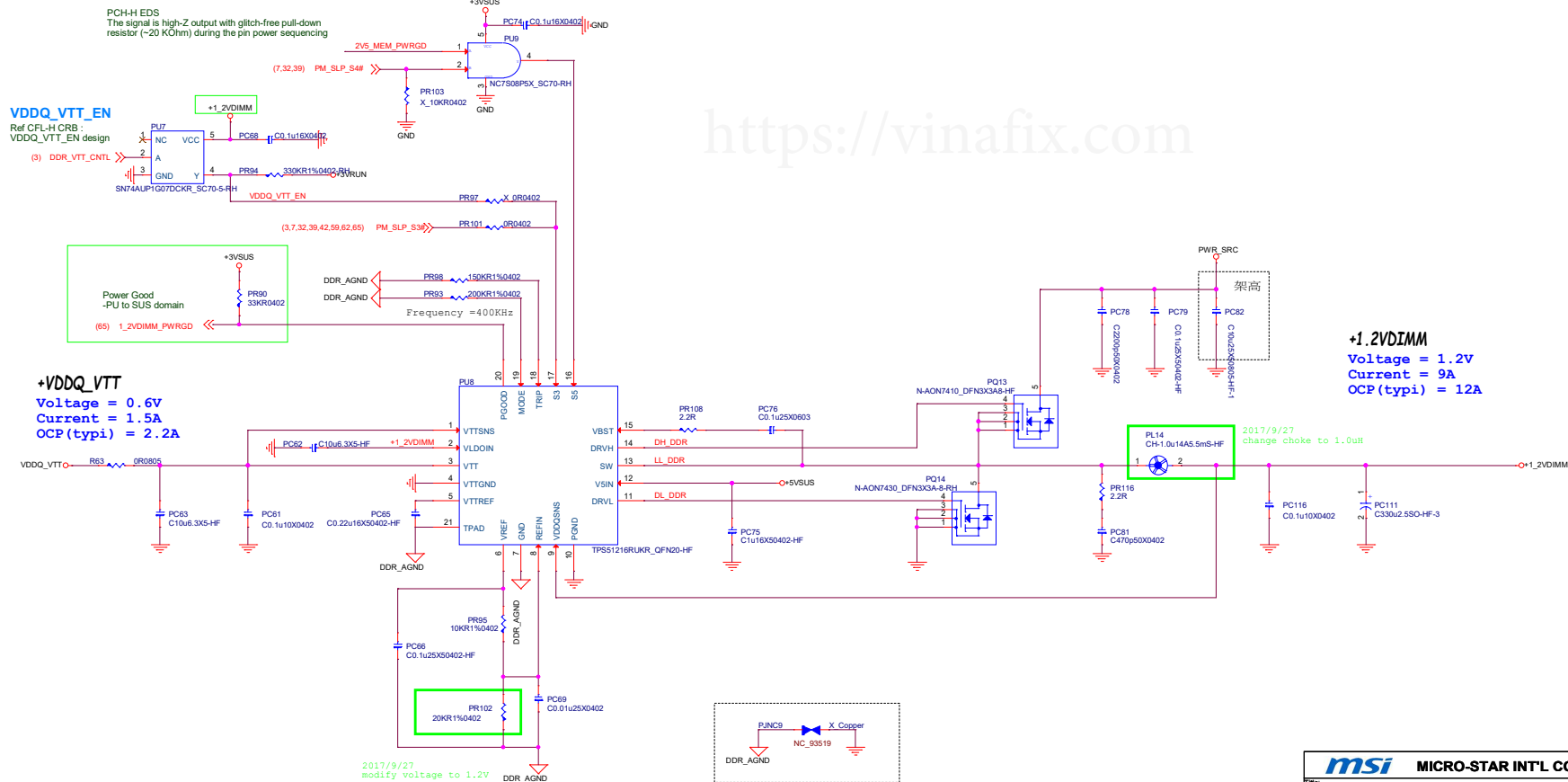




## +2.5V\_MEM (DDR4/Vpp)

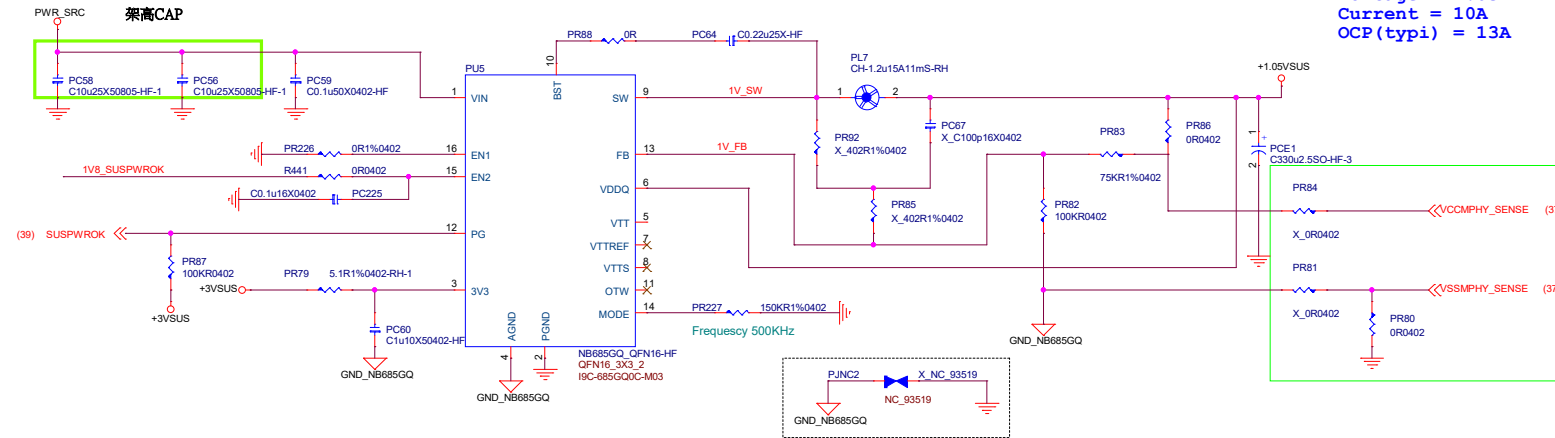


## +1.2VDIMM / VDDQ\_VTT(0.6V)

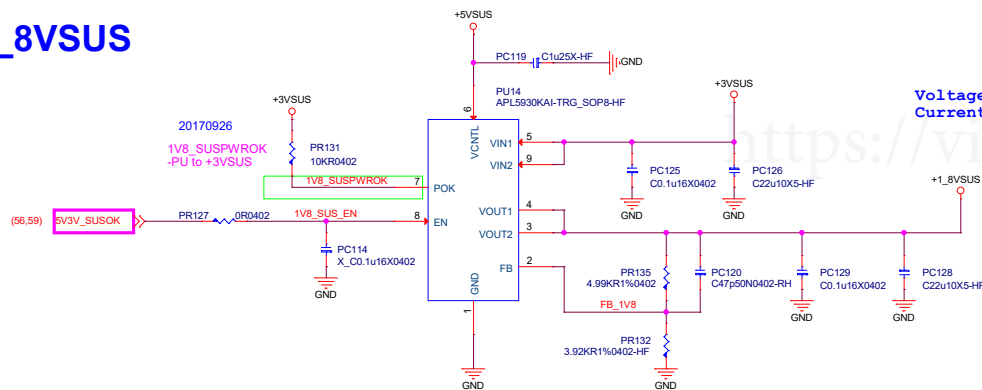




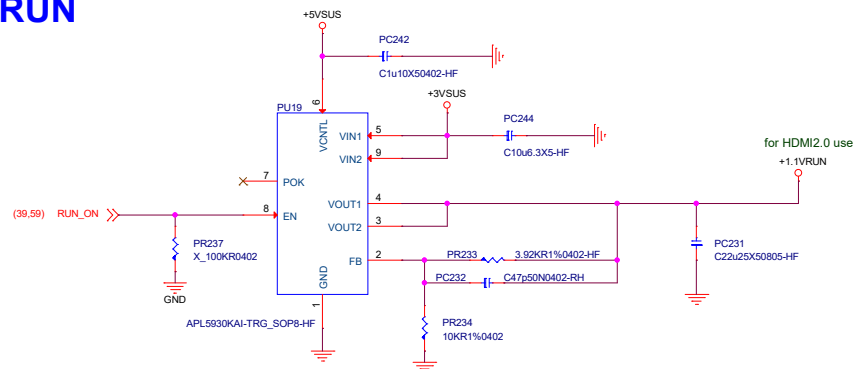
## +1.05VSUS



## +1\_8VSUS

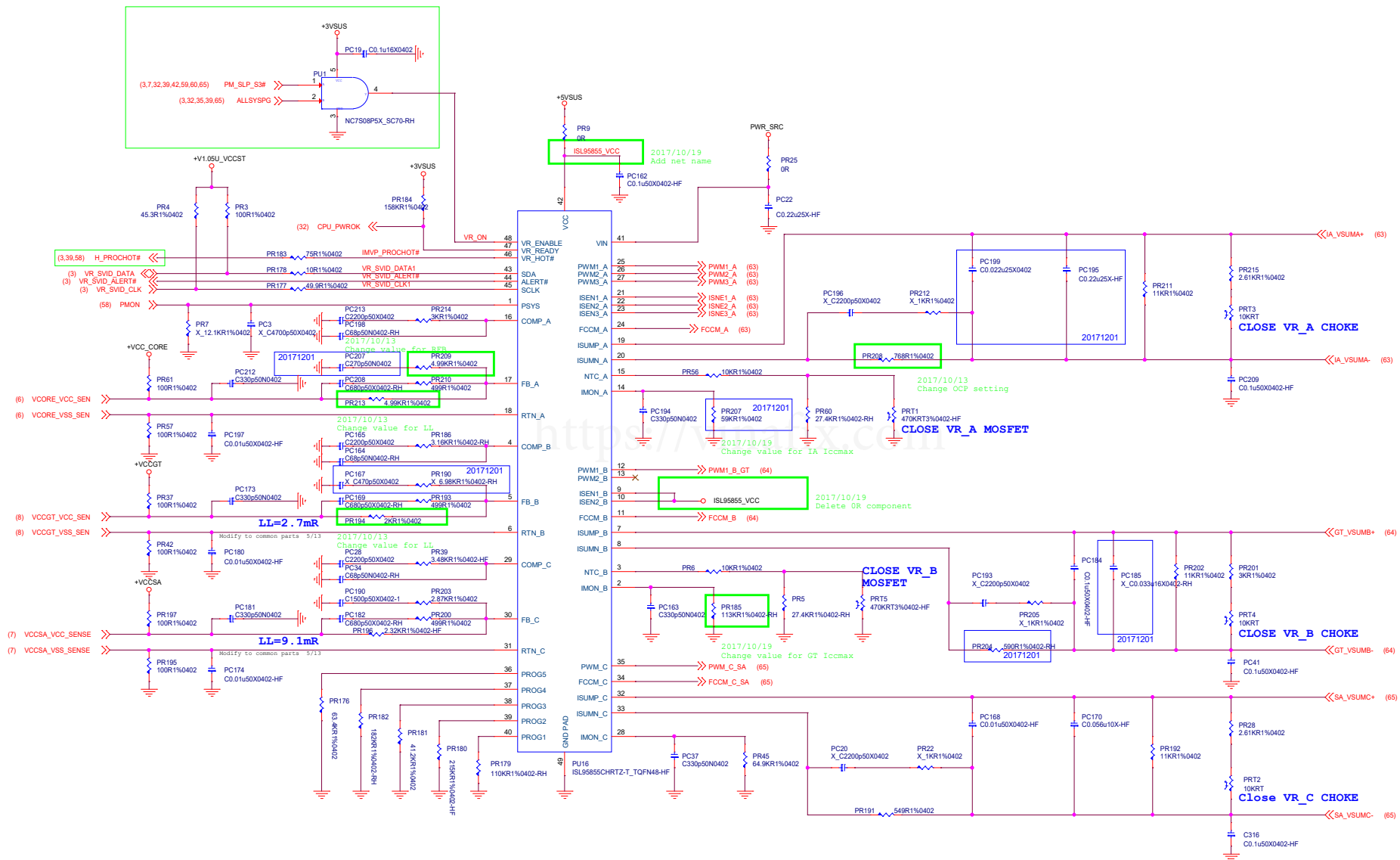


## +1.1VRUN





*Coffee Lake H-line*  
6+2 45W ISL95855C

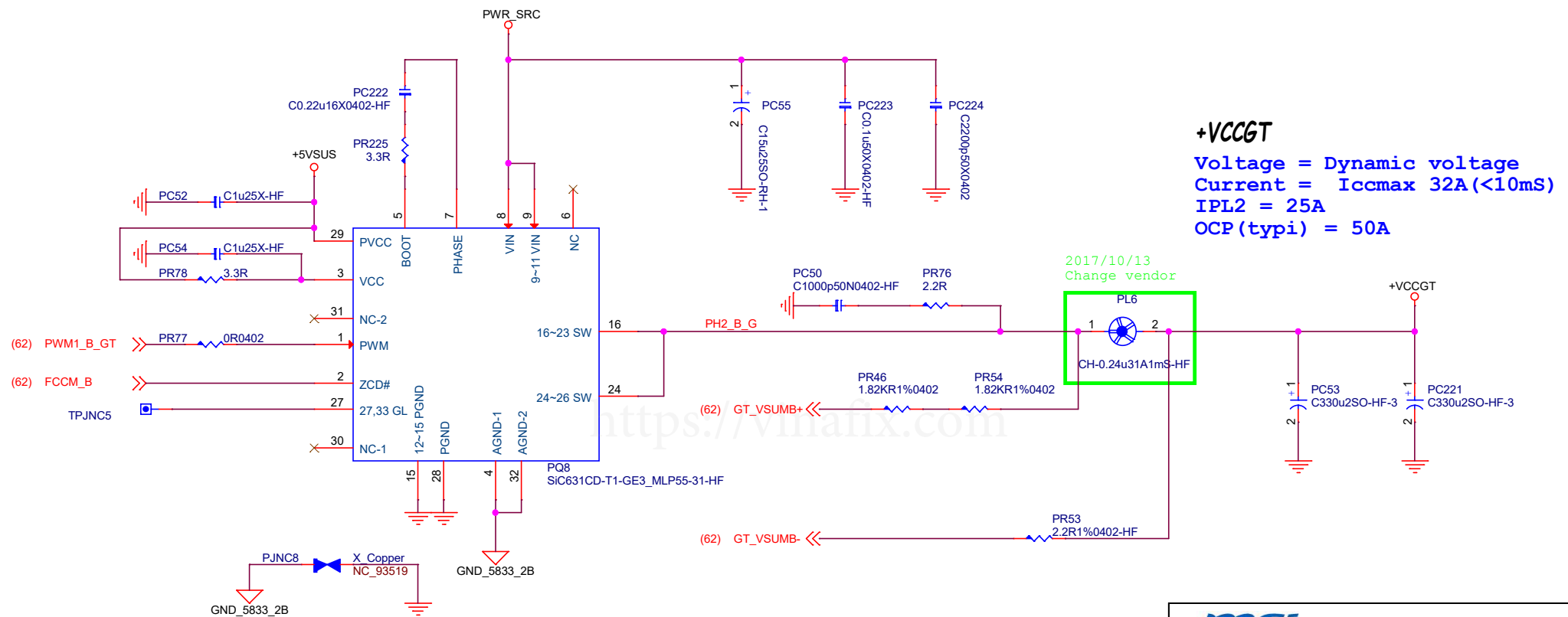









**+VCCGT**



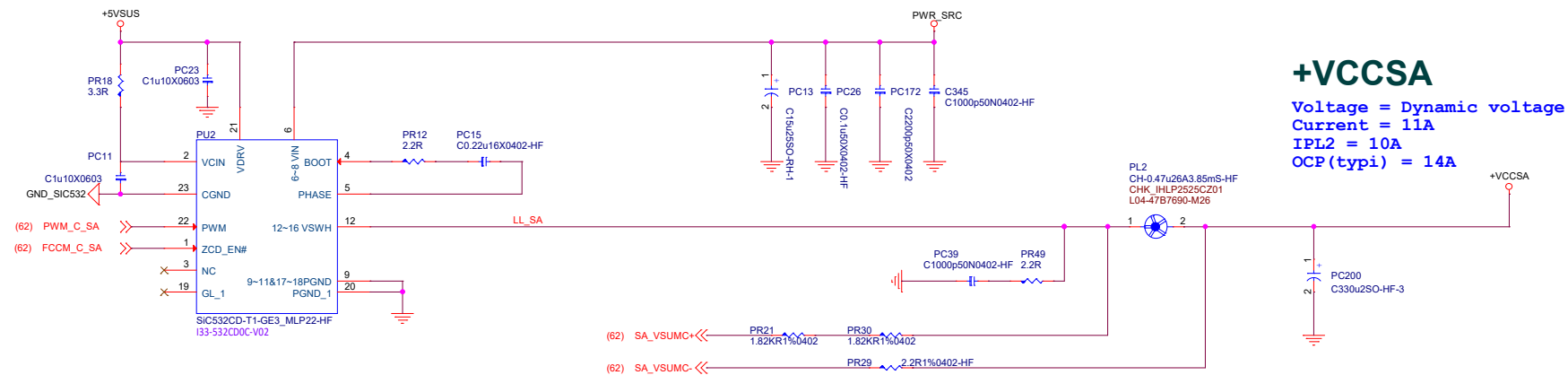
**+VCCGT**

Voltage = Dynamic voltage  
Current = Iccmax 32A(<10mS)  
IPL2 = 25A  
OCP(typi) = 50A

 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>VCCGT</b>	
Size	Document Number
Custom	<b>MS-16Q2</b>
Date:	Thursday, January 25, 2018
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## +VCCSA

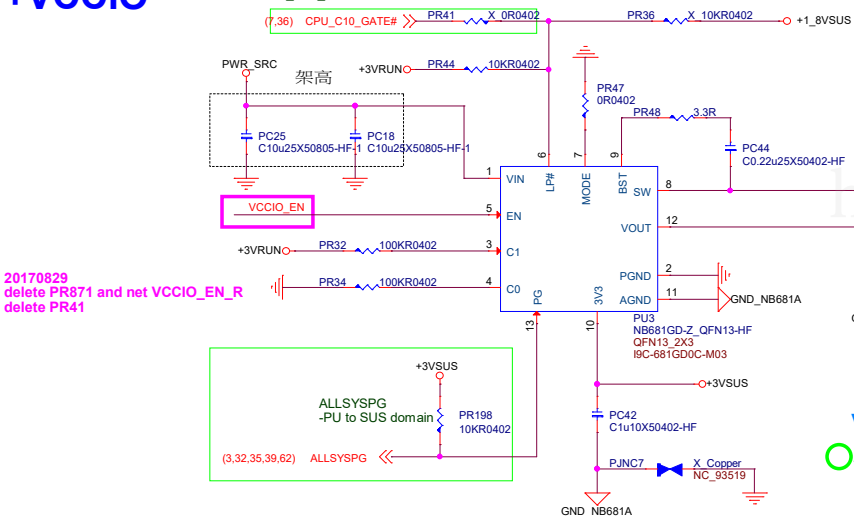


## +VCCSA

Voltage = Dynamic voltage  
Current = 11A  
IPL2 = 10A  
OCP(typi) = 14A

## +VCCIO

Power Sequence spec ICPU27 :  
CPU\_C10\_GATE# de-assertion to VCCSTG stable 10 < tCPU26 < 240 us

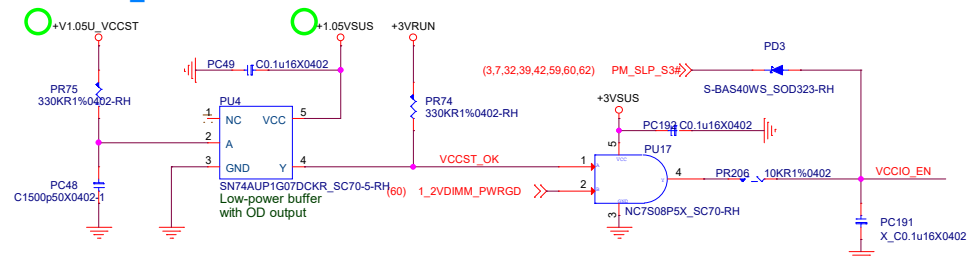


## +VCCIO

Voltage = 0.95V  
Current = 5.5A  
OCP(typi) = 7.5A

Vinafix.com

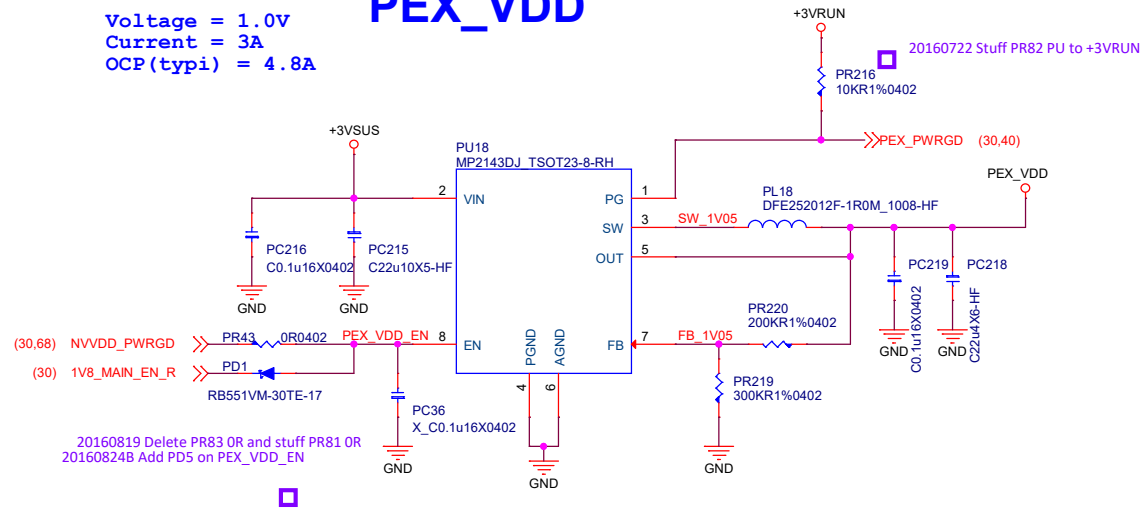
## VCCIO\_EN





Voltage = 1.0V  
Current = 3A  
OCP (typi) = 4.8A

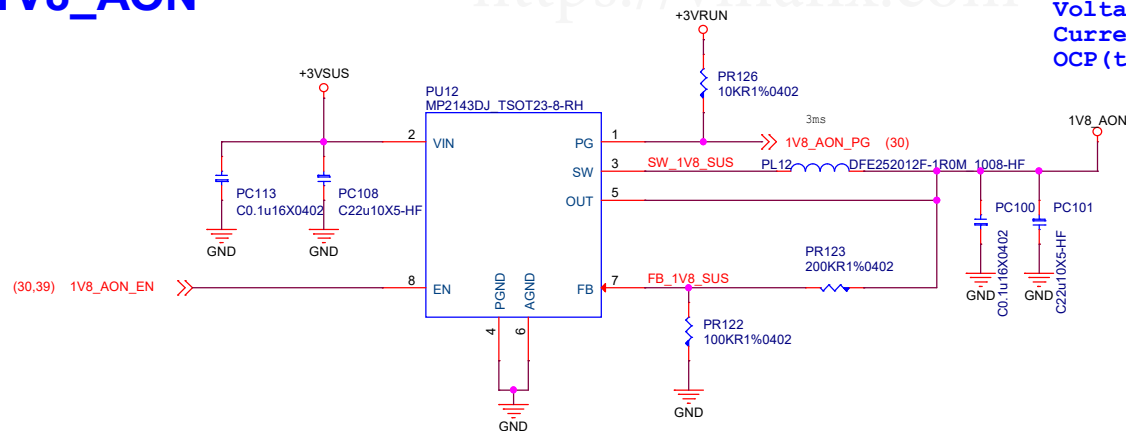
## PEX\_VDD



## 1V8\_AON

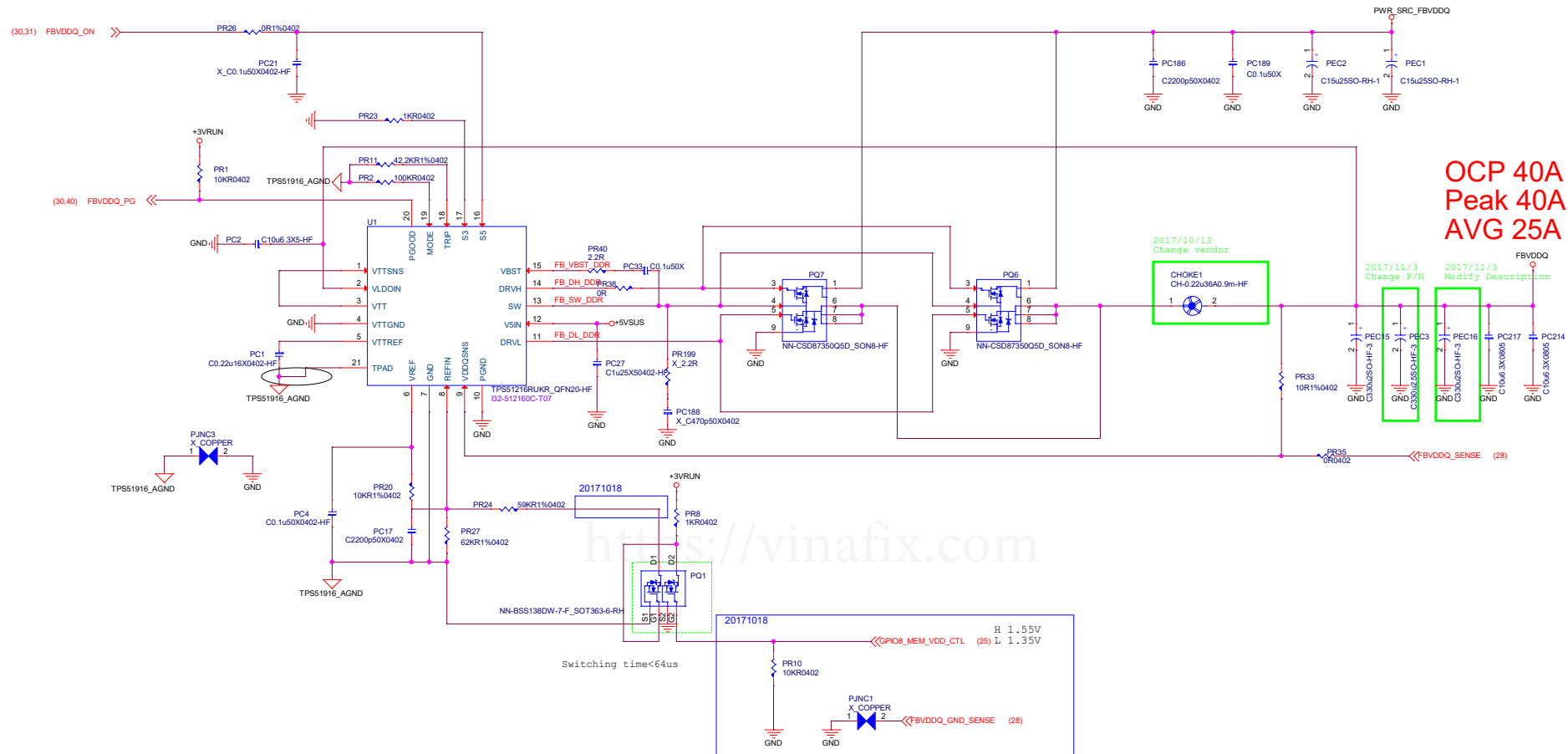
### 1V8\_AON

Voltage = 1.8V  
Current = 2.26A  
OCP (typi) = 4.8A



<b>msi</b> MICRO-STAR INT'L CO.,LTD.	
Title	
<b>1V8_AON/PEX_VDD</b>	
Size	Document Number
B	<b>MS-16Q2</b>
Date:	Thursday, January 25, 2018
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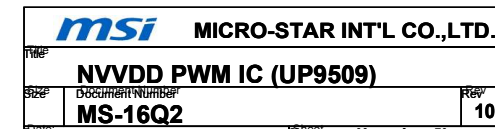






## EDP-Con 80A

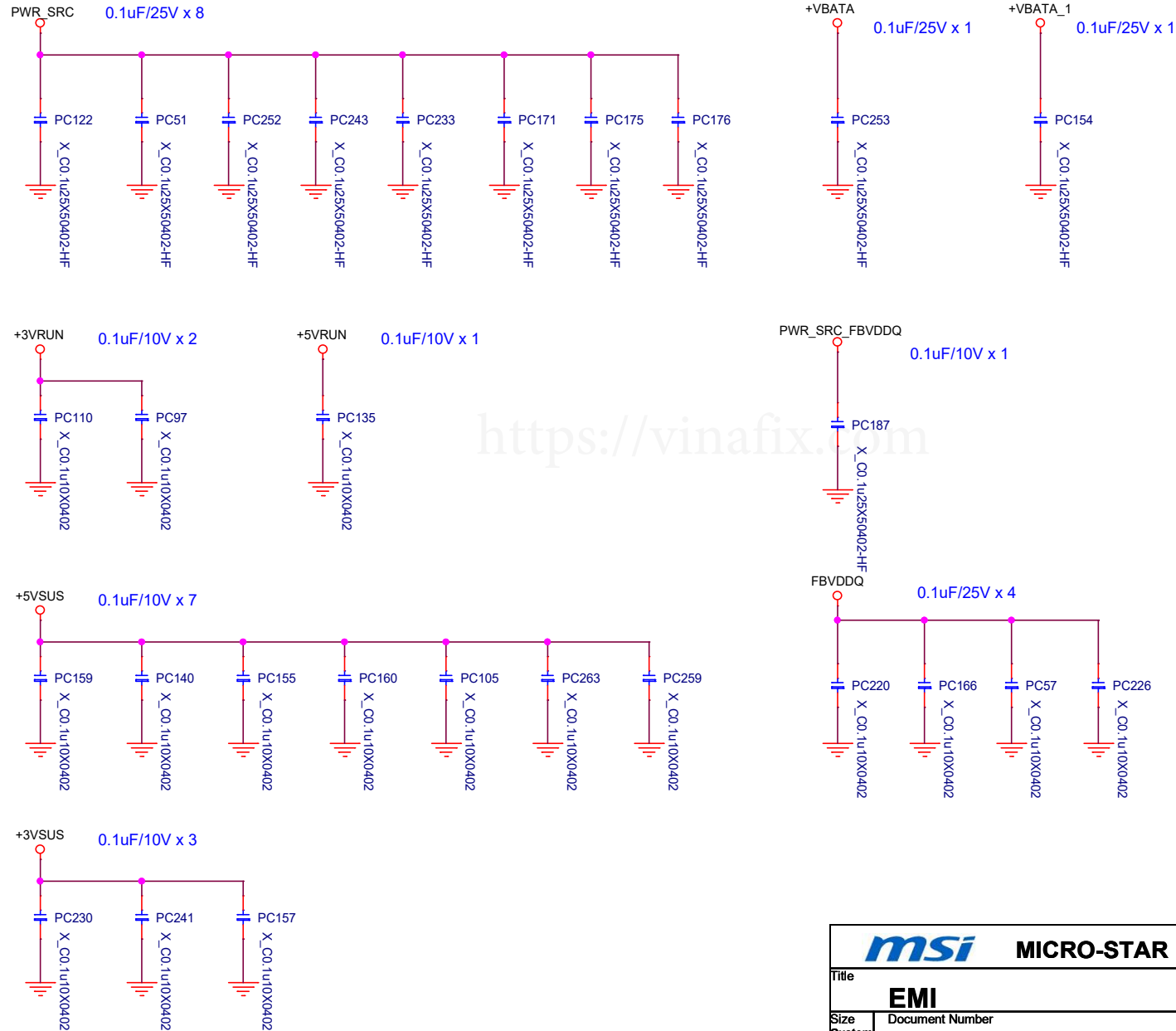
**Vmin:0.3V / Vmax:1.3V**





# EMI

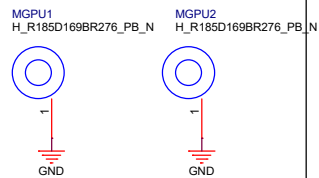
20171018



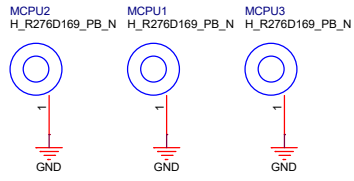
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Title	
<b>EMI</b>	
Size	Document Number
Custom	<b>MS-16Q2</b>
Date:	Thursday, January 25, 2018
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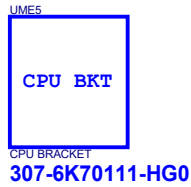
## dGPU Holes



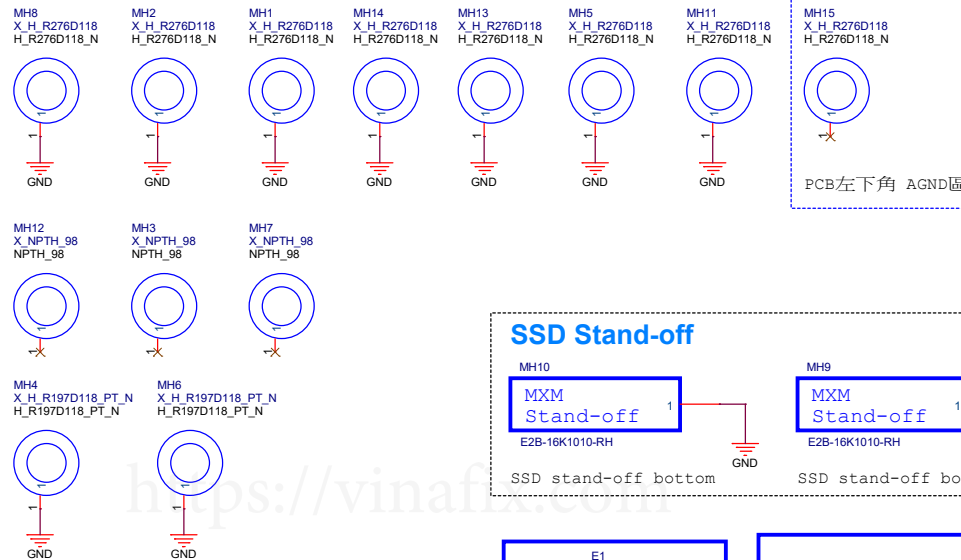
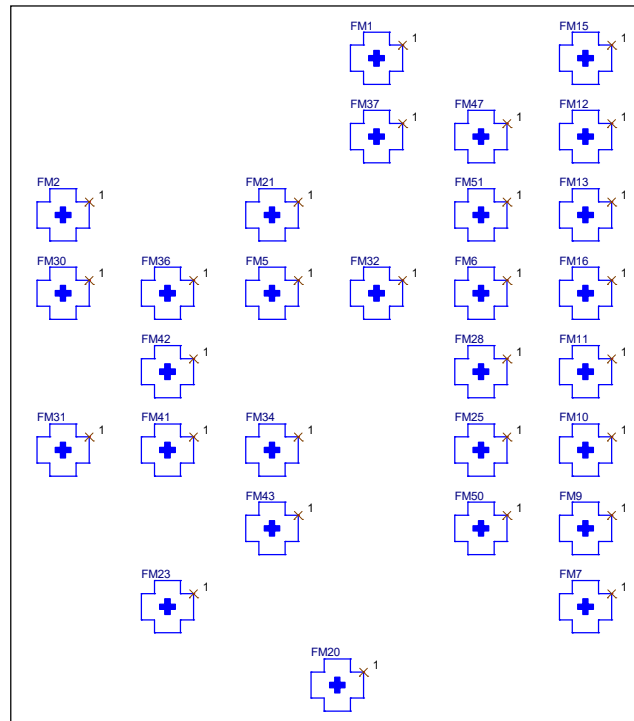
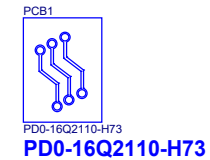
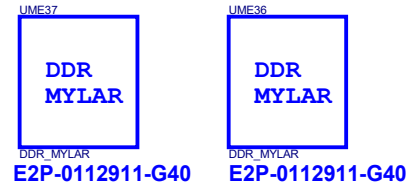
## CPU Holes



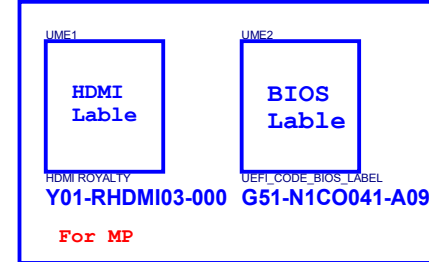
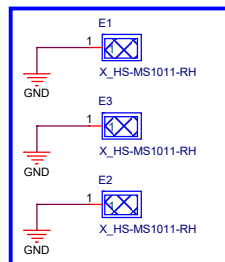
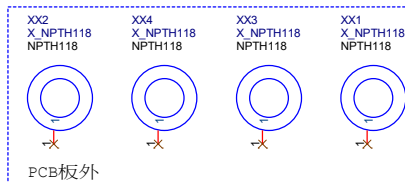
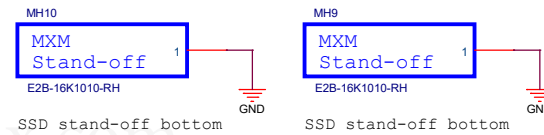
## BKT



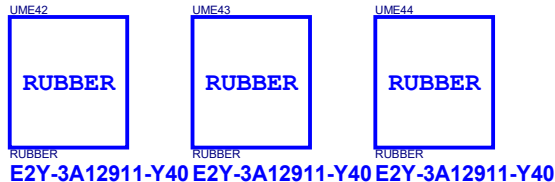
## MYLAR



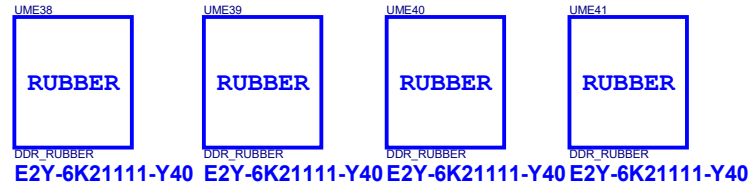
## SSD Stand-off



## RUBBER



## DDR RUBBER



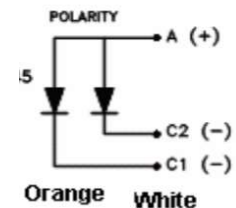
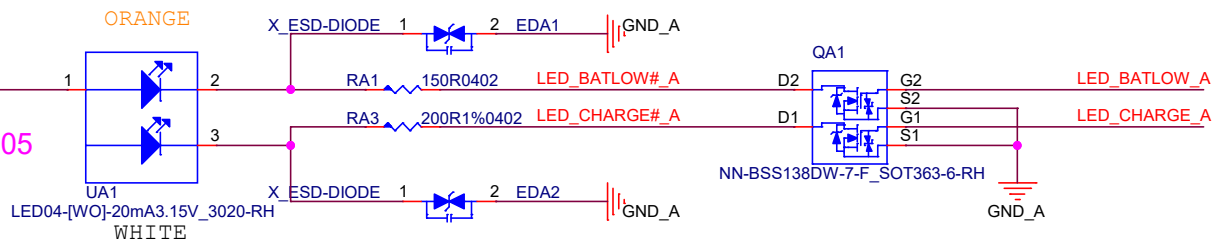
## ADHESIVE\_TYPE



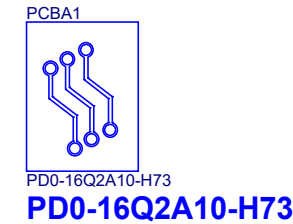
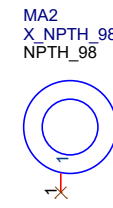
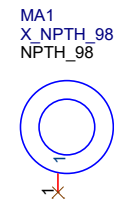
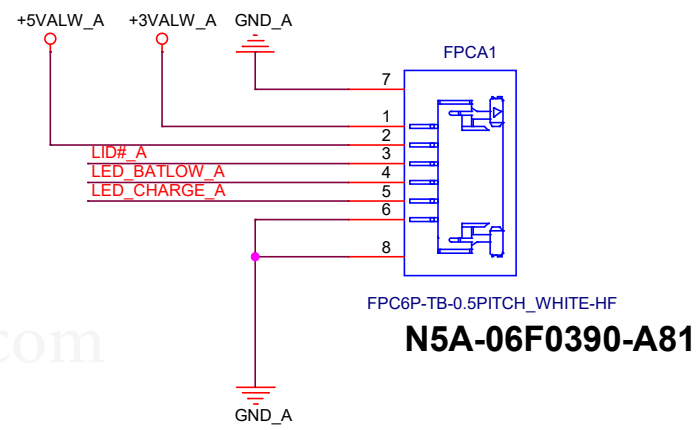
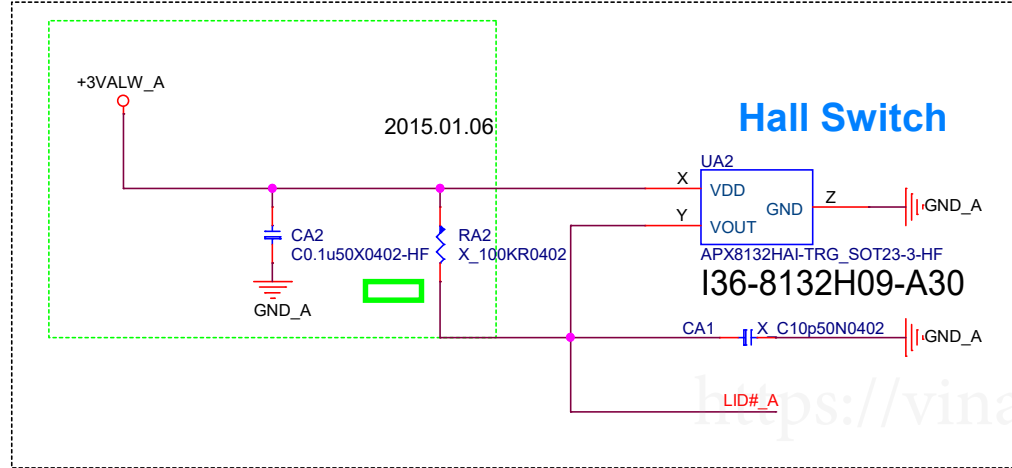



+5VALW\_A

D0C-040M700-L05



Part No.	Lens	Emitted Color	Pin Assignment
LTW-326DSKF-5A	Yellow	InGaN White	C2
		AlInGaP Orange	C1



**MICRO-STAR INT'L CO.,LTD.**

**Title**  
**LED / Hall Switch**

<b>Size</b> Custom	<b>Document Number</b> <b>MS-16Q2</b>	<b>Rev</b> <b>10</b>
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Ref #543611 Chapter40  
Figure 40-4. SKL-S Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]  
Table 40-5. Platform Sequencing Timing Parameters



Ref #543611 Chapter40  
Figure 40-6. SKL-S Timing Diagram for S0 to G3 [Non-Deep  
Sx Platform]  
Table 40-5. Platform Sequencing Timing Parameters





History

16Q2 10

DATE	PAGE	DESCRIPTION	DATE	PAGE	DESCRIPTION	DATE	PAGE	DESCRIPTION	DATE	PAGE	DESCRIPTION
20171005	ALL	first version from 16Q2									
	32	Unstuff R616 (PCH-LP Only)									
	58	Unstuff PR30289(H_PROCHOT#)									
	70	Modify ME/Screw									
	56	Modify USB to N53-09M1071-AF2									
	48,50	Modify 22R/0201 to 22R/0402									
20171012	55	Unstuff R100 for CRB									
	39,50	R10271/R10272 move to EC side for Vendor.									
	2	power on block (DIMM_ON_2V5)									
	50	Remove C10229									
	47	Modify U10033(ALC1220) to B05-012203C-R09									
20171016	48	Set POR1 to High for Vendor.									
	22	1V8_MAIN add C10865(1uF/0402) for Nvidia check.									
	26	VID_PLLVDD add C10866(4.7uF/0402) for Nvidia check.									
	24	PEX_VDD add C10867(1uF/0402) for Nvidia check.									
	22	1V8_MAIN add C10868(0.1uF/0402) &C10869(4.7uF/0402) for Nvidia check.									
		NVVDD add PEC30005(330uF) for Nvidia check.									
	45	FPC PIN Swap for FP Con.									
	56	Modify ESD for USB3.1 Layout.									
	46	Remover R10566/R10570 for Layout.									
20171017	41	EL10007 pin swap for Layout.									
	40	Add PEX_PWRGD for Nvidia check.									
20171018	67	Remove R/C for Power									
	69	Add EMI Cap for EMI									
20171019	69	Modify EMI Cap for EMI									
	56	Modify power circuit for power .									
		Add 10uF/0402 for Vendor .									
20171020	63	Remove PC151 for Power									
	41	Add C30320 for EMI									
20171023	All	Rename									
20171024	All	Rename Con.									
20171025	All	ALC1220 change to B05-012204C-R09(VB2)									
		SSC_EN pull High for Asmedia.									
20171030	All	0A BOM									
20171201	59	Unstuff PEC4									
	62	Stuff PEC14									
		Modify PC195 to C11-2242633-W08(0.22uF)									
		Modify PC199 to C11-2232032-W08(0.022uF)									
		Unstuff PC185, PC167, PR190									
		Modify PC207 to C11-2711022-W08(270pF)									
		Modify PR207 to R11-0593T12-W08(59K-ohm)									
		Modify PR204 to R11-0591T12-W08(590-ohm)									
	63	Unstuff PC206									
		Stuff PC203									
20171204	All	Modify D03-65D8L09-D07 to D03-138DW19-D07									
		(PQ1,PQ2,PQ23,PQ29,PQ34,Q2,Q8,Q34,Q35,Q36,Q38,Q40,Q43,Q46,Q63,QA1)									
	48	Stuff R646 , unstuff R650 for Audio Vendor.									
	9,10	Modify C982,C1008 to C71-331037E-P01 for ME									
	45	Unstuff SW1 for ME									
	9,10	Stuff C946,C1036 for SA									
	62	Modify PR184 to R11-1583T12-W08 for Sequence									
	32	Modify C132 to C11-1057412-Y01 for Sequence									
	47	Modify C1219,C1220 to C11-2267313-M09 for Audio									
	32	Remove BAT2									
20171207	32	Stuff R122 for Sequence									
		Unstuff R128 for Sequence									
	66	Modify PD1 to D01-RB55120-R06									
20180102	40	Stuff R199									
	49	Stuff R188 , unstuff R189									
	68	Stuff PC134									
		Modify PR152 to R11-0621T12-W08									
20180103	10	Swap RTC1									
	56	BAT2 change to D06-0105701-K26									
		Add C1245-C1248 for SA,(USB Eye)									
		Remove EL6,EL7,R364,R365 for Asmedia.									
	32,39	Add EC_PCHPWROK for power sequence.									
	31	Modify PC132,PC136,PC148,PC149 to C11-1067620-M09(0805).									
	41	Add R690(100K) for Panel Flicker issue.									
	3-8	Modify U4(CPU) to OAD-16K5004-I06(QS I7-8750H).									
	32-38	Modify U13(PCH) to OB1-16K5002-I06 (HM370(QNWF)).									
20180104	60	PJNC9 Change to NC_93519 for layout									
20180111	34	PCIE17-20 Change to PCIE21-24									
	34,46	Remove M2_SSD2_PDET									
	46	Swap PCIE2_M2_RX17N & PCIE2_M2_RX17P									
20180111	70,71	PCB Ver. 1.0									
	71	RA3 Change to R11-0201T12-W08(200 ohm)									
	47	Stuff C237									
	70	Add RUBBER*3 (E2Y-3A12911-Y40) for ME									
		Add DDR_RUBBER*4 (E2Y-6K21111-Y40) for ME									
		Add ADHESIVE_TYPE*1 (E2Y-8121911-G40) for ME									
20180125	42	U28 Change to B07-L634015-I06									